THE ELECTRONICS RESURGENCE INITIATIVE

DISTRIBUTION STATEMENT A: Approved for public release.

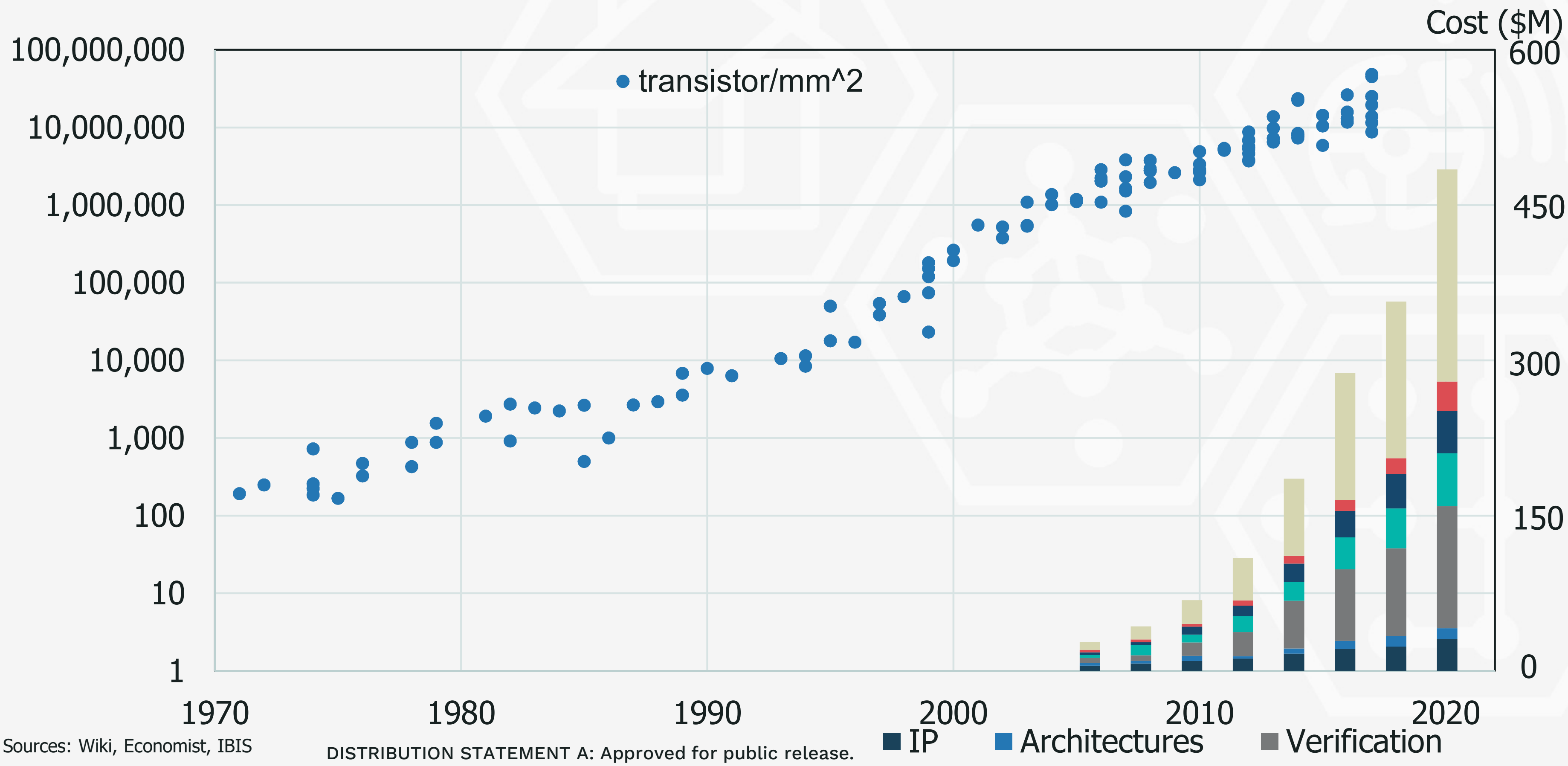
ANDREAS OLOFSSON

PROGRAM MANAGER
DARPA, MTO

DARPA IS BUILDING A SILICON COMPILER

ANDREAS OLOFSSON
PROGRAM MANAGER
DARPA/MTO

WE ARE LOSING THE COMPLEXITY BATTLE



Sources: Wiki, Economist, IBIS

DISTRIBUTION STATEMENT A: Approved for public release.

DARPA'S $100M HARDWARE COMPILER INVESTMENT

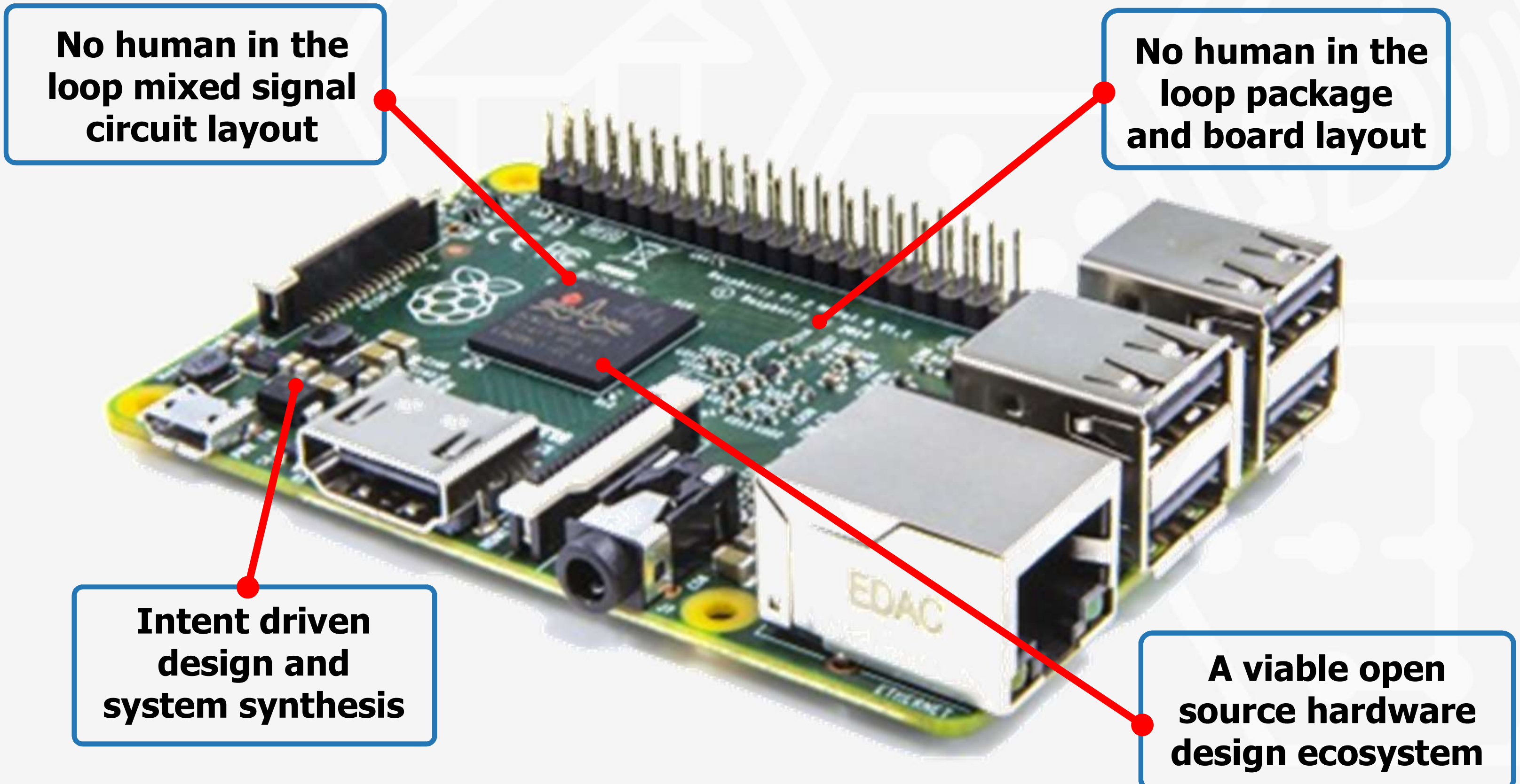


Image Source: Raspberry Pi

END STATE – THE FIRST GENERAL PURPOSE SILICON COMPILER

```
$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42
```

Image Sources: Amazon, NVIDIA

SELECTED PROGRAM PARTICIPANTS

Academic Partners

University of California at San Diego

University of Michigan

Purdue

Carnegie Mellon University

Boston University

Stanford

University of Washington

Princeton University

University of Illinois at Urbana Champaign

Purdue University

Brown University

Yale

University of Southern California

University of Utah

U of Minnesota

University of Texas at Dallas

Cairo University

University of Virginia

Commercial Partners

Synopsys

Cadence Design Systems

Intel

ARM

Qualcomm

Xilinx

NVIDIA

Analog Devices

Northrop Grumman

JITX

Lockheed Martin

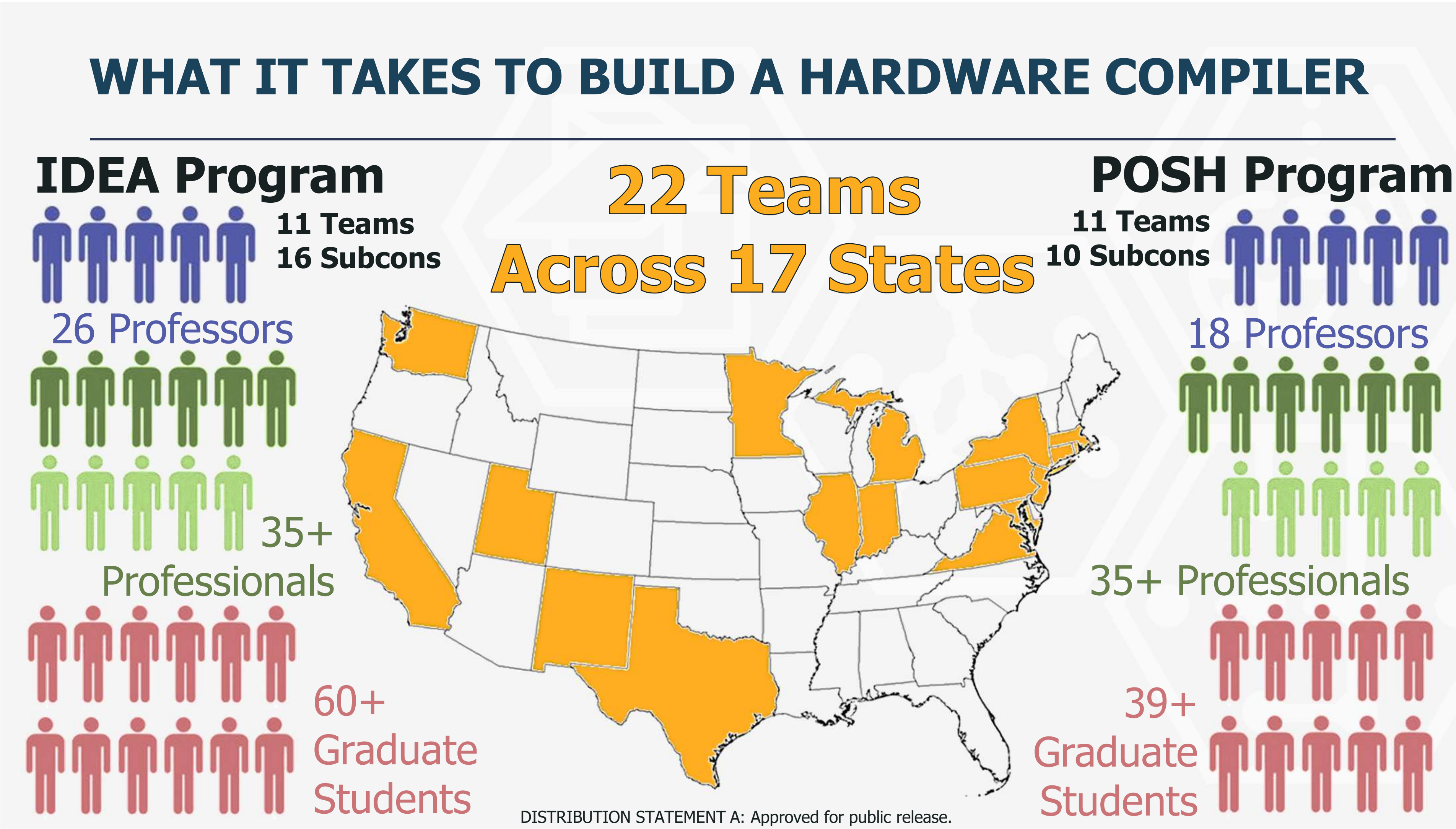
Global Foundries

MOSIS

Analog Circuit Works

LeWiz

Sandia National Laboratories


WHAT IT TAKES TO BUILD A HARDWARE COMPILER
IDEA Program
11 Teams
16 Subcons
26 Professors
35+ Professionals
60+ Graduate Students
22 Teams
Across 17 States
POSH Program
11 Teams
10 Subcons
18 Professors
35+ Professionals
39+ Graduate Students
DISTRIBUTION STATEMENT A: Approved for public release.

SAMPLE OF PROGRAM RESEARCH EFFORTS

Cadence Design Systems
Analog Layout

Yale
Asynchronous Design

Synopsys
Mixed Signal Emulation

University of Washington
Open source analog IP

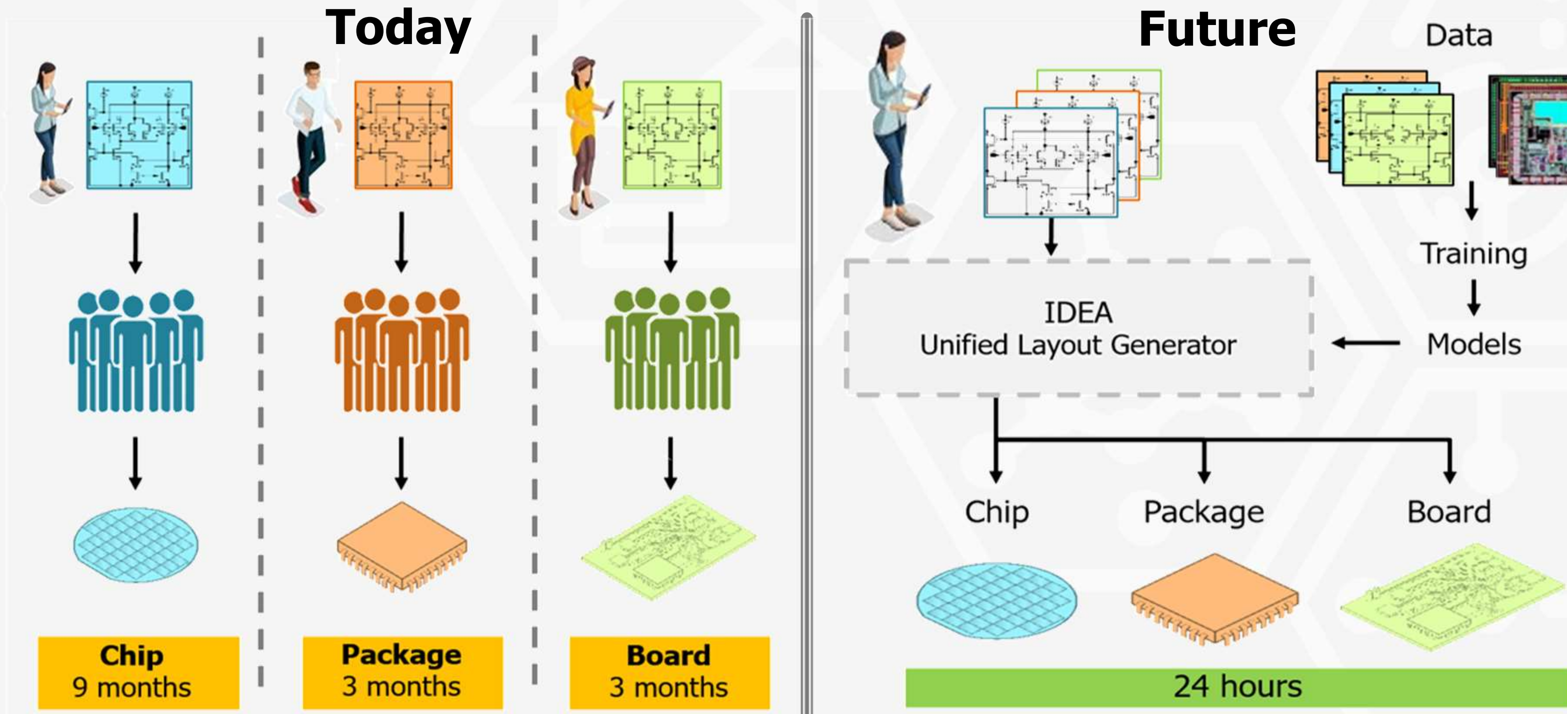
University of California at San Diego
Digital Layout

University of Washington
RISC-V

NG/JITX
Design by intent

Xilinx
Mixed HW/SW Emulation

IDEA: A UNIFIED ELECTRICAL CIRCUIT LAYOUT GENERATOR



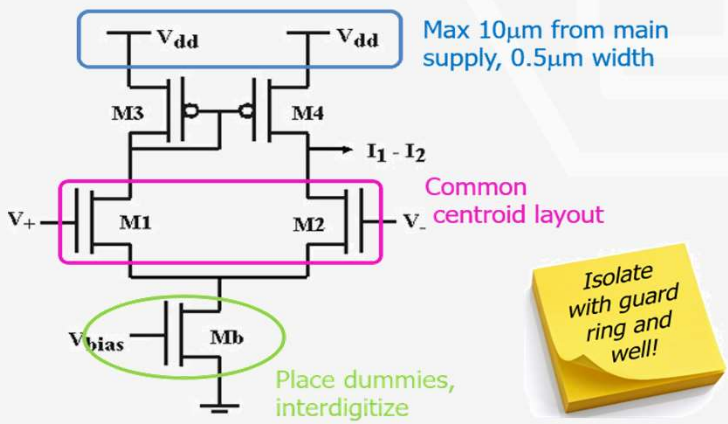
- Knowledge embedded in humans
- Limited knowledge reuse
- Reliance on scarce resources

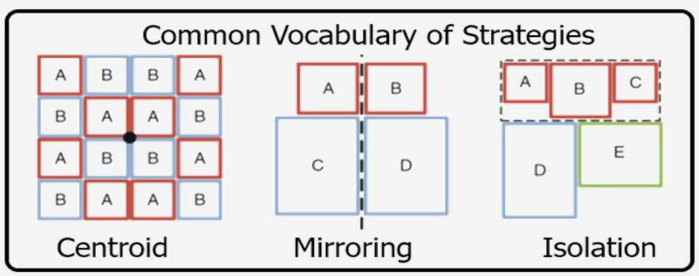
- Knowledge embedded in software
- 100% automated hardware compilation
- 24 hour turnaround

IDEA: NO HUMAN IN THE LOOP DIGITAL AND ANALOG LAYOUT!

Today

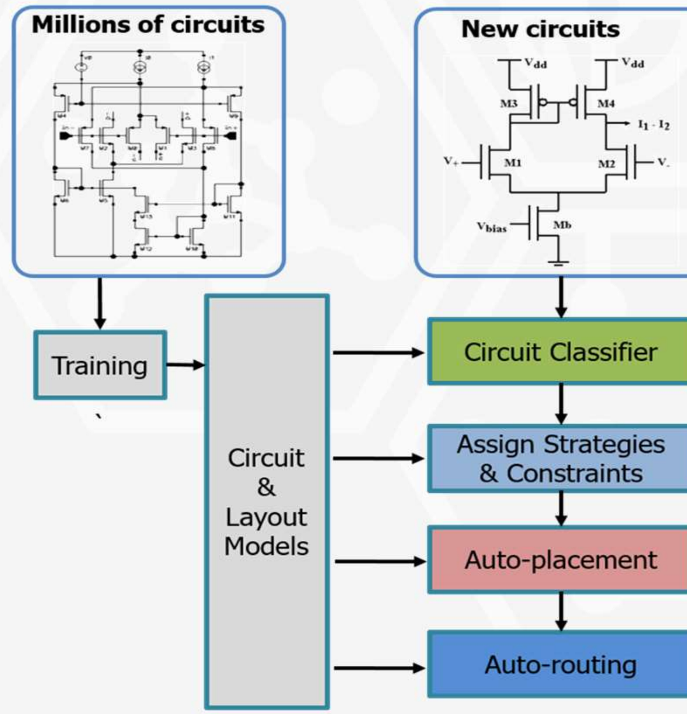
Designer provides manual constraints to layout person (or tool)





Future

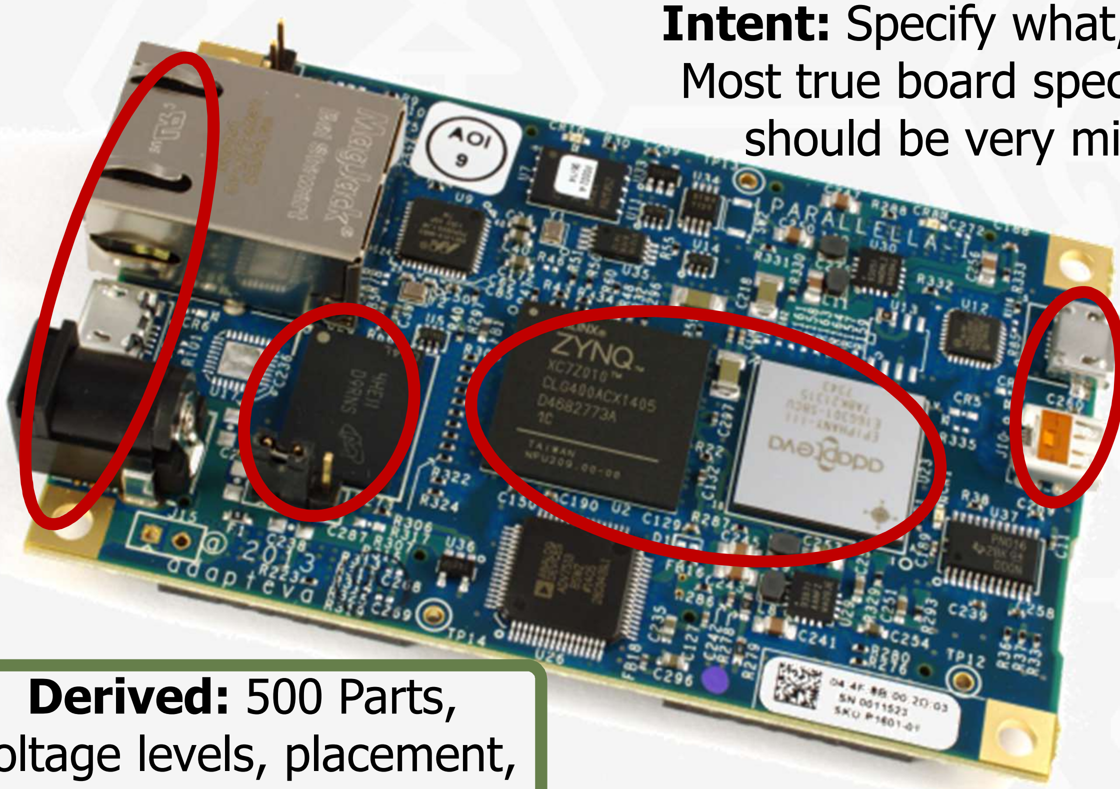
Automatically assign constraints based on trained circuit & layout models



IDEA: INTENT-DRIVEN SYSTEM SYNTHESIS

True Specs:
5V
Ethernet
USB
HDMI
1GB RAM
128MB Flash
FPGPA
20 GFLOPS
ARM A9

Intent: Specify what, not how!
Most true board specifications should be very minimal.

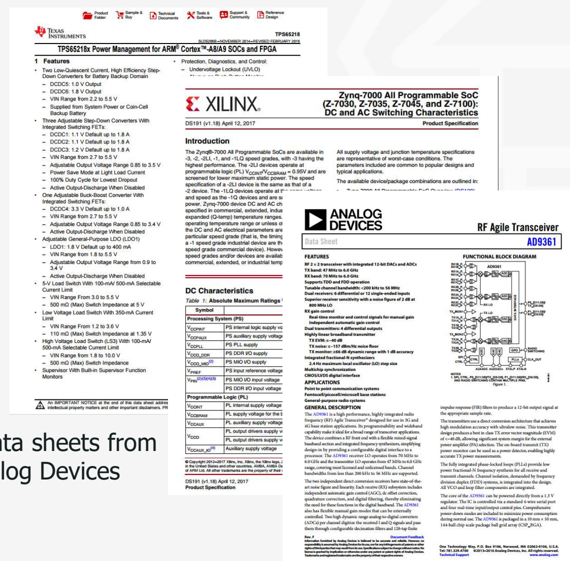


Derived: 500 Parts, voltage levels, placement, routing, connectivity

Image source: Adapteva

IDEA: AN OPEN 5M+ COMPONENT IC DATABASE

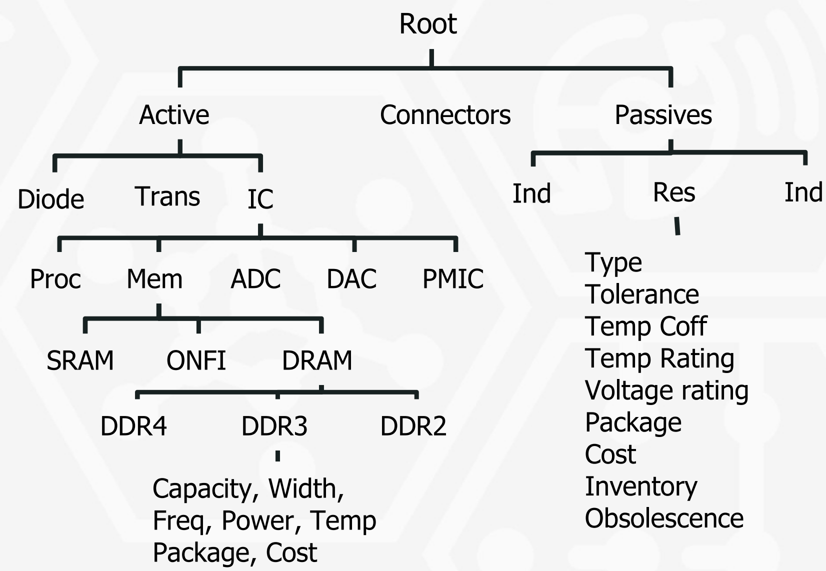
Today



Source: data sheets from Xilinx, Analog Devices

- 5M+ parts in circulation
- Information embedded in datasheets and reference designs
- No standard models
- Automatic optimization not possible

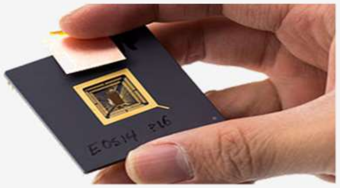
IDEA



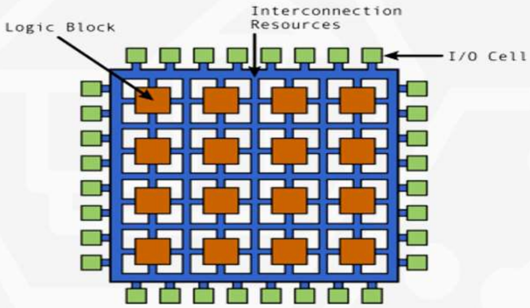
- IC standard models (LEF,LIB,IP-XACT)
- Extend standards for boards / SIPs
- Creation of 5M+ part DB
- <u>Model all properties needed for constraint-based system optimization</u>

POSH: EXPECTED PROGRAM RESULTS

RISC-V

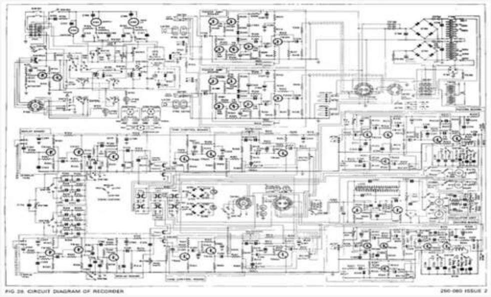


Multicore RISC-V

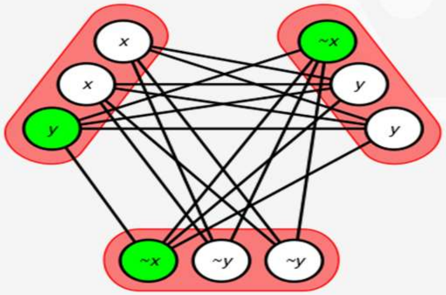


Open source FPGA Chips

"Linux for SoC Design"



Open source analog IP



Signoff level validation

Commercial open source design community

Image sources: Farhek, Wikipedia, EE Times

SILICON COMPILER PROGRAM SCHEDULE

```
$ git clone https://github.com/darpa/idea
$ git clone https://github.com/darpa/posh
$ cd posh
$ make soc42
```

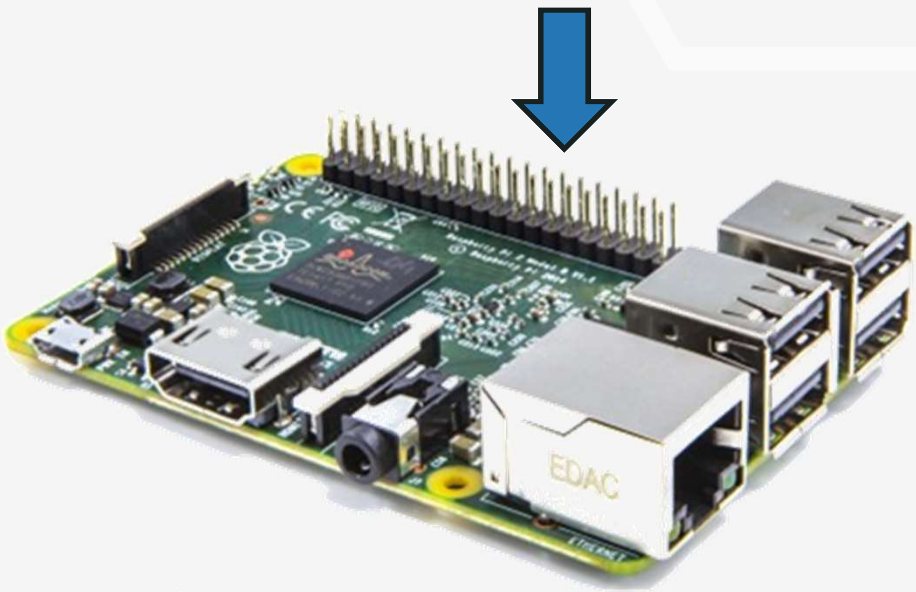


Image Source: Raspberry Pi

2018	• Program Kickoff
2018	• First Integration Exercise
2019	• Alpha Release, working code
2020	• Working Beta Silicon Compiler • 50% PPA
2022	• Program Completion • 100% PPA

TIME

Time	Distance
1 ns	Foot
1 us	Eiffel Tower
1 ms	NY to Boston

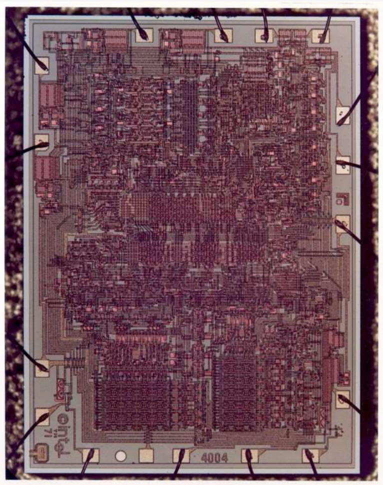
Image Source: U.S. Naval History

GRAVITY

Real time machine learning?

Image Sources: Drone Air, IBM

SPACE



- Original Intel 4004
- 2,300 transistors
- Fits in a cell at 3nm?

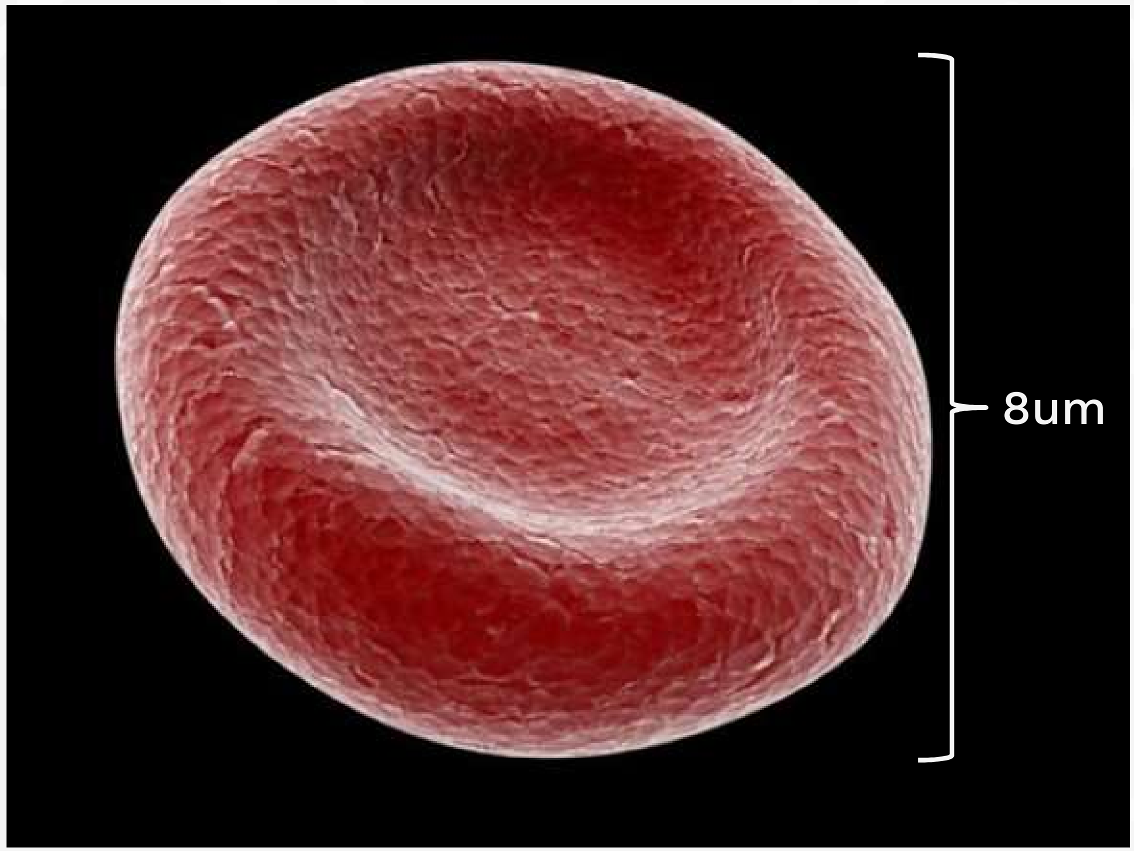


Image Sources: Intel, CGTrader

THE ELECTRONICS RESURGENCE INITIATIVE

DAVID WHITE

SR. DIRECTOR R&D, CADENCE

cādence®

MAGESTIC: MACHINE LEARNING FOR AUTOMATIC GENERATION OF ELECTRONIC SYSTEMS THROUGH INTELLIGENT COLLABORATION

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA)

cādence® WHO WE ARE

Cadence provides leading electronic design automation (EDA) software and hardware for chip, package, board, and system design as well as semiconductor intellectual property

7,200+ employees

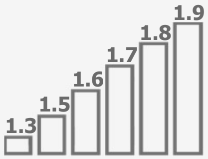
21 countries

NEW

20 new products and 50+ new IP products in the past 3 years

FORTUNE 100 BEST COMPANIES TO WORK FOR 2017

Q4 FY17 revenue: $502M



FY12 – 17 Revenue ($B)

$804M in R&D investment in 2017

40% of revenue invested in R&D

Broad portfolio of electronics design and IP products

OUR SOLUTIONS

- CHIP (Core EDA)
- PACKAGE AND BOARD
- SYSTEM INTEGRATION

KEY MARKETS

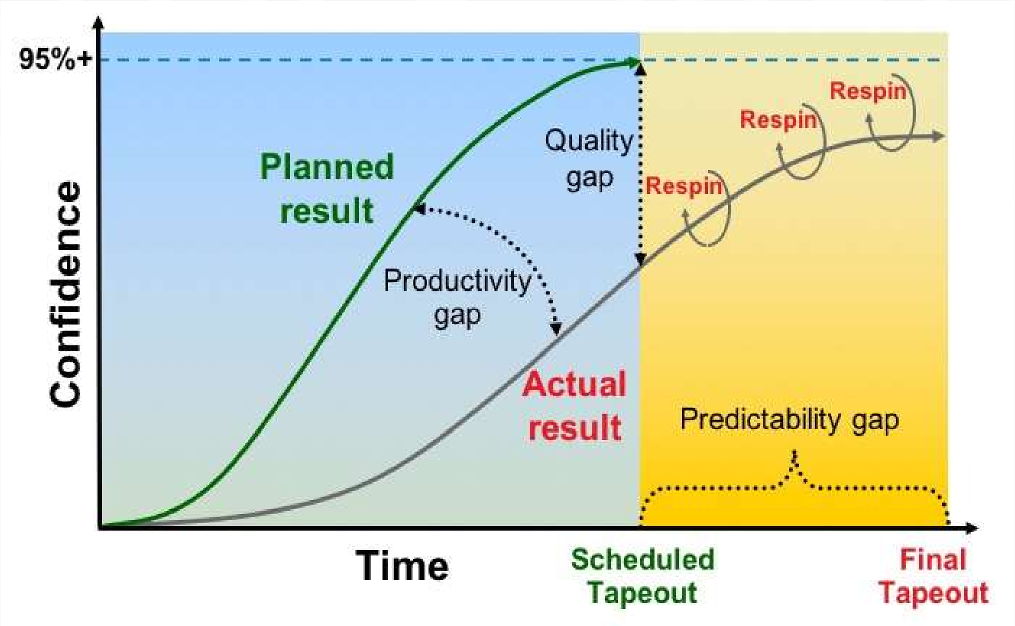
- AERO/DEF
- MOBILE
- AUTOMOTIVE
- MEDICAL
- DATACENTER
- AND MORE...

Distribution Statement A- Approved for Public Release, Distribution Unlimited

CHALLENGES TO PRODUCTIVITY IN DESIGN TODAY

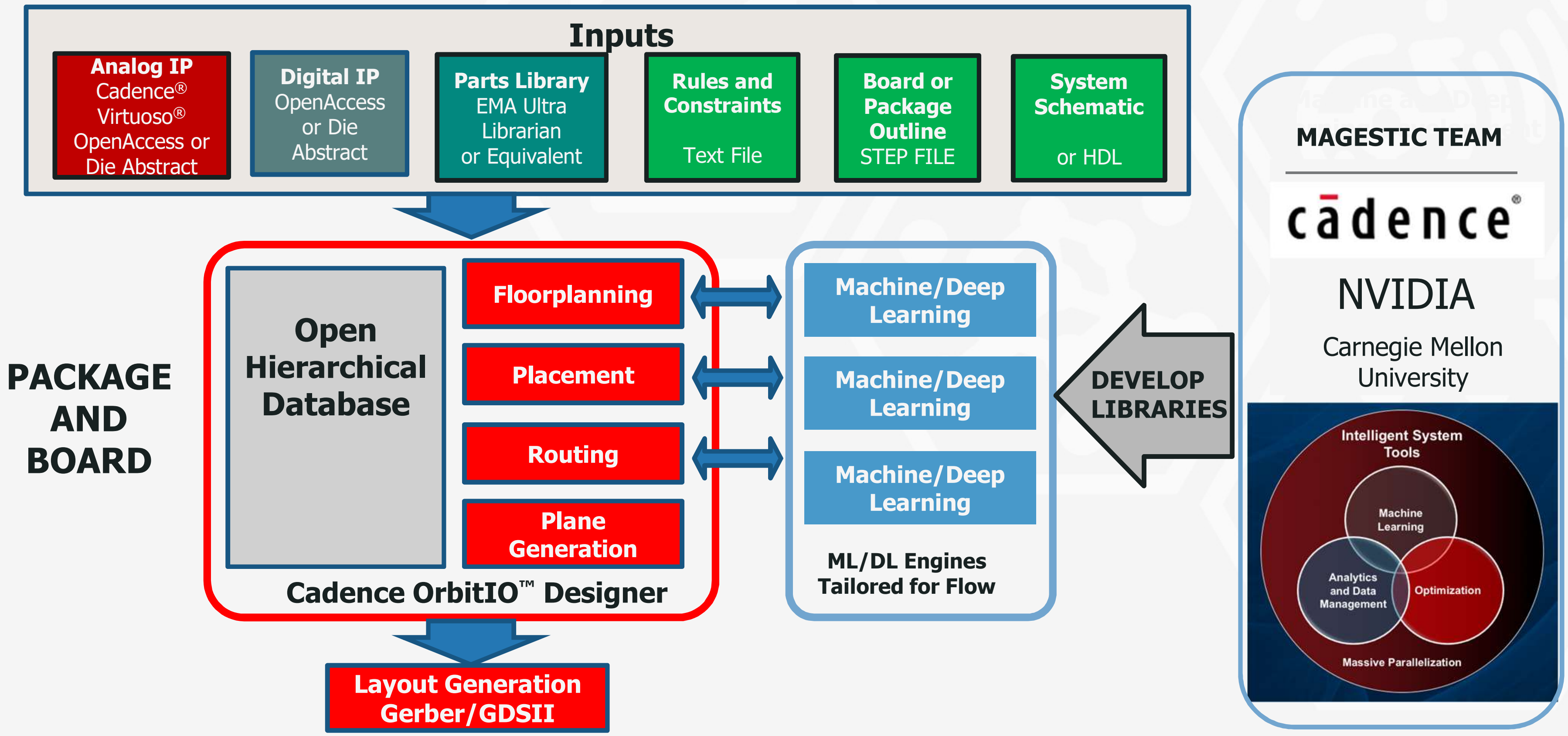
Respins increase cost of electronics

- IDEA MAGESTIC will:
  - Improve productivity
  - Reduce design costs
  - Improve electronics
  - Reliability
  - Performance
  - Power



cādence®

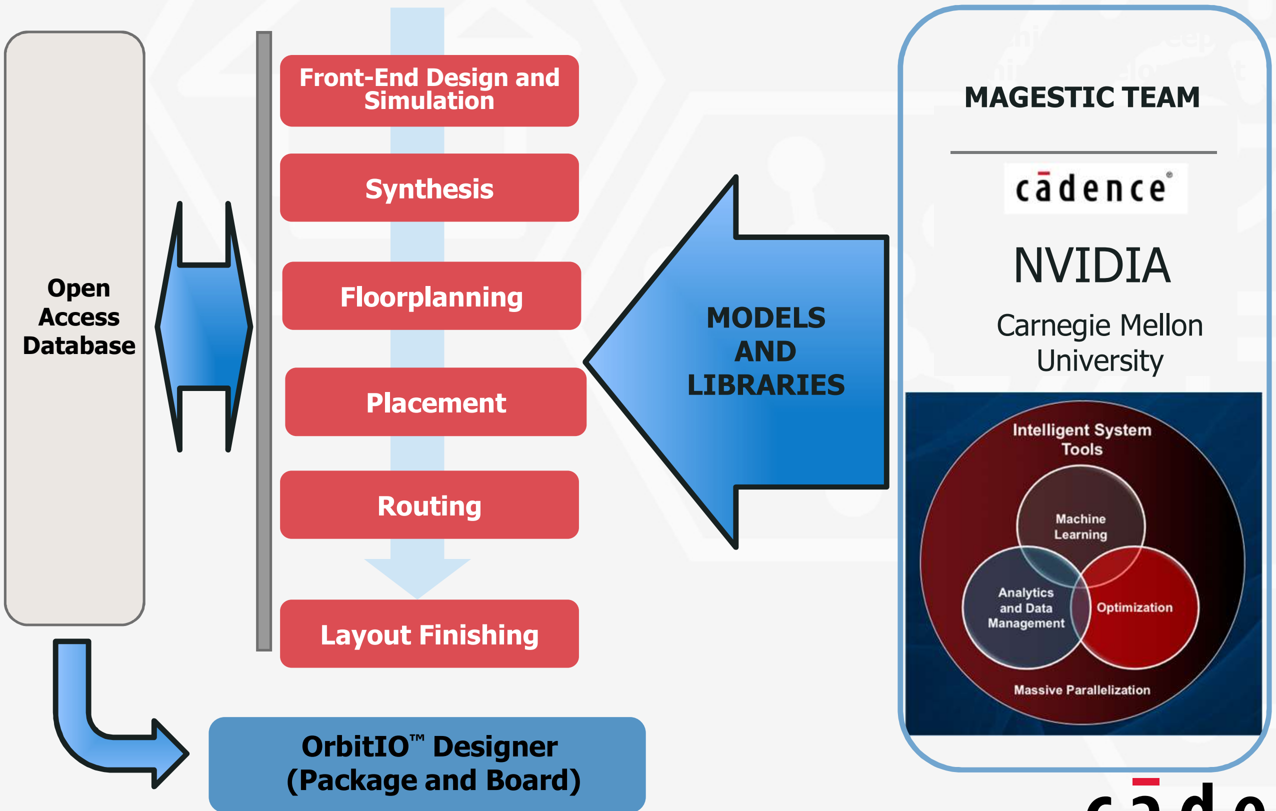
MAGESTIC FLOW USES MACHINE/DEEP LEARNING



INTELLIGENT DESIGN FLOW FOR CUSTOM ICS

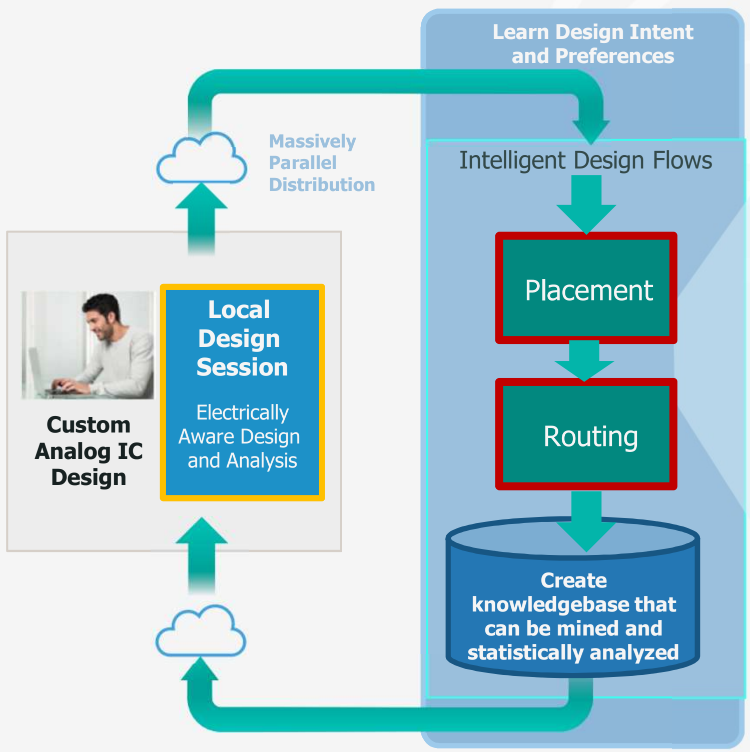
IDEA goals:

- Cloud enabled
- No human in loop
- <24-hr TAT
- Acceptable quality of results



cadence®

ML-BASED PLACEMENT OF CUSTOM IC DESIGN

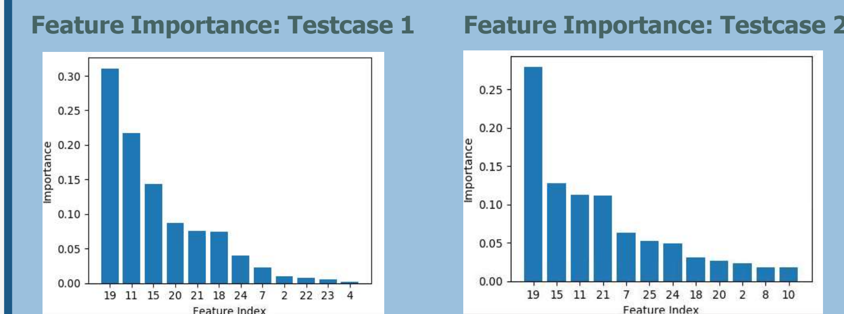


Uses ML/DL Technology

*layout images are for demonstration purposes only

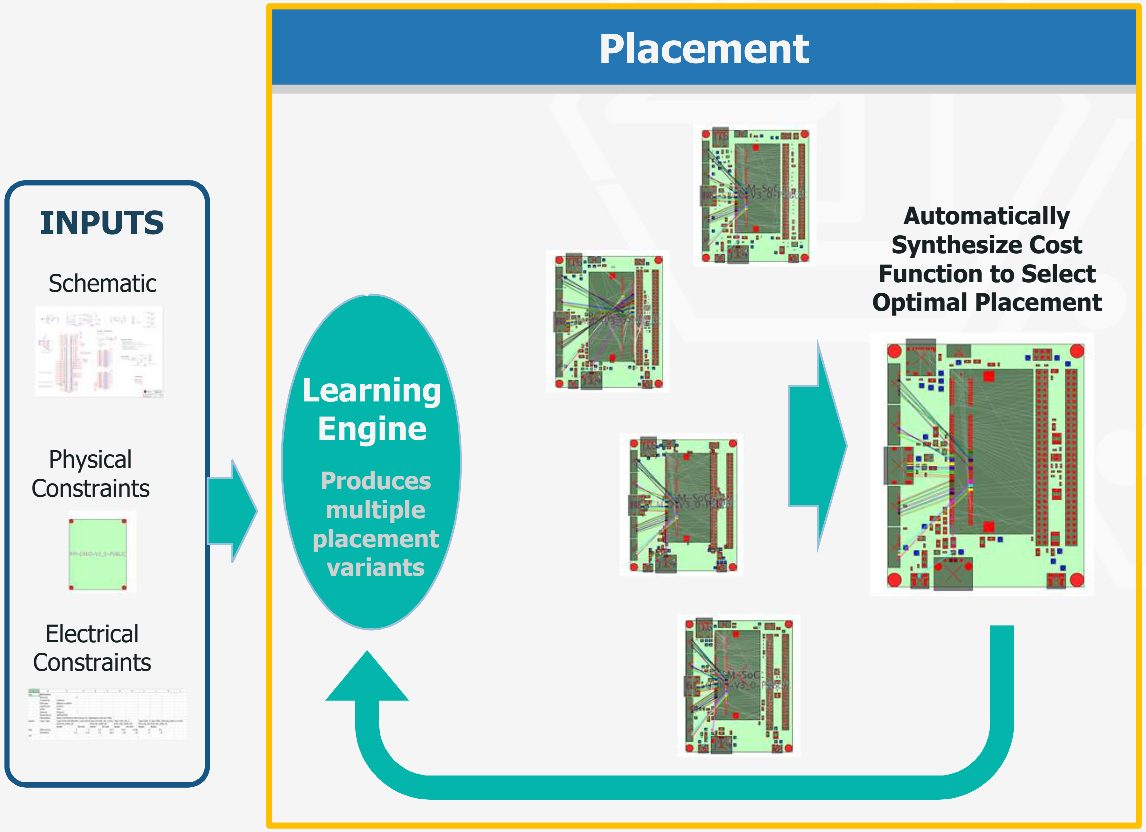
Test / Train	1	2
1	100%	97.7%
2	91.0%	100%

Feature Importance Extracted from Testcase Structures



Developing ML solutions to automatically extract most relevant layout features

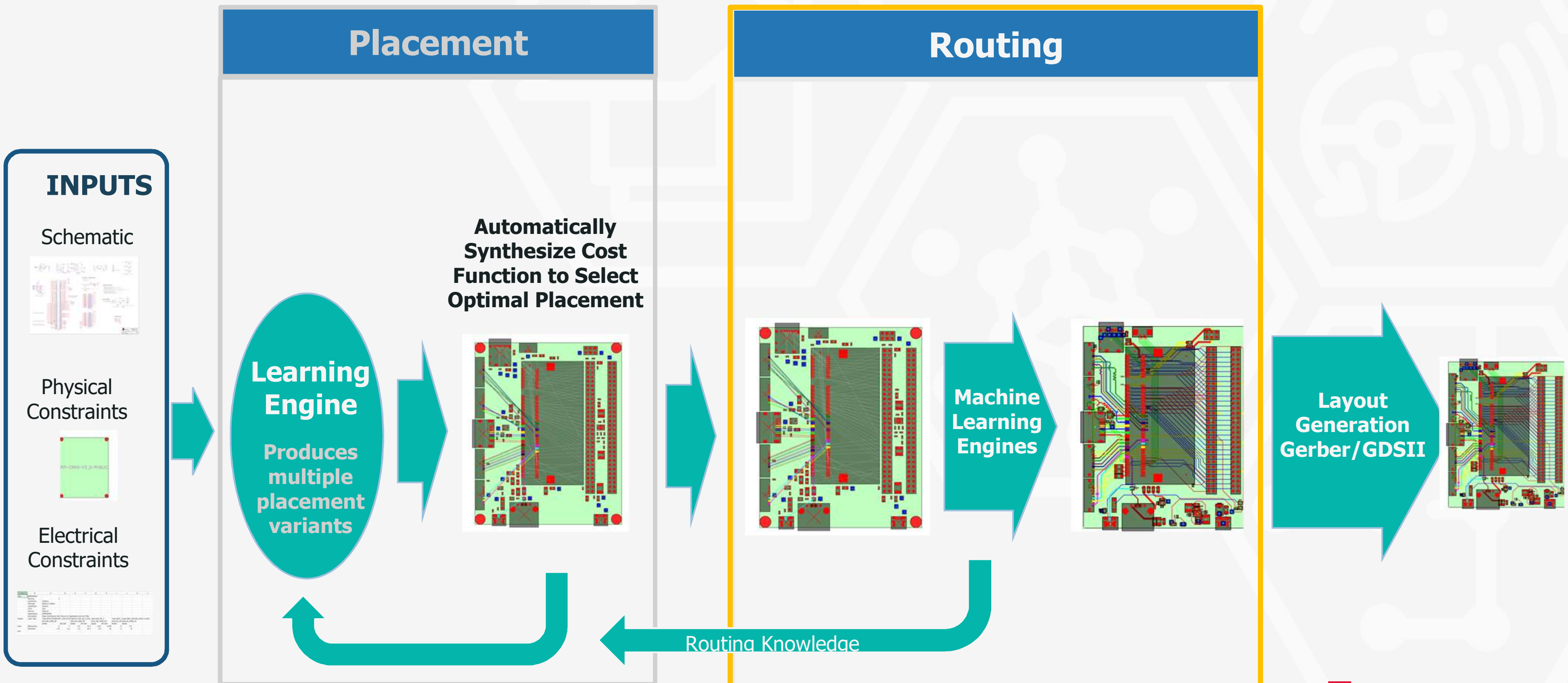
DEEP LEARNING-BASED AUTOMATIC PLACEMENT OF PCB



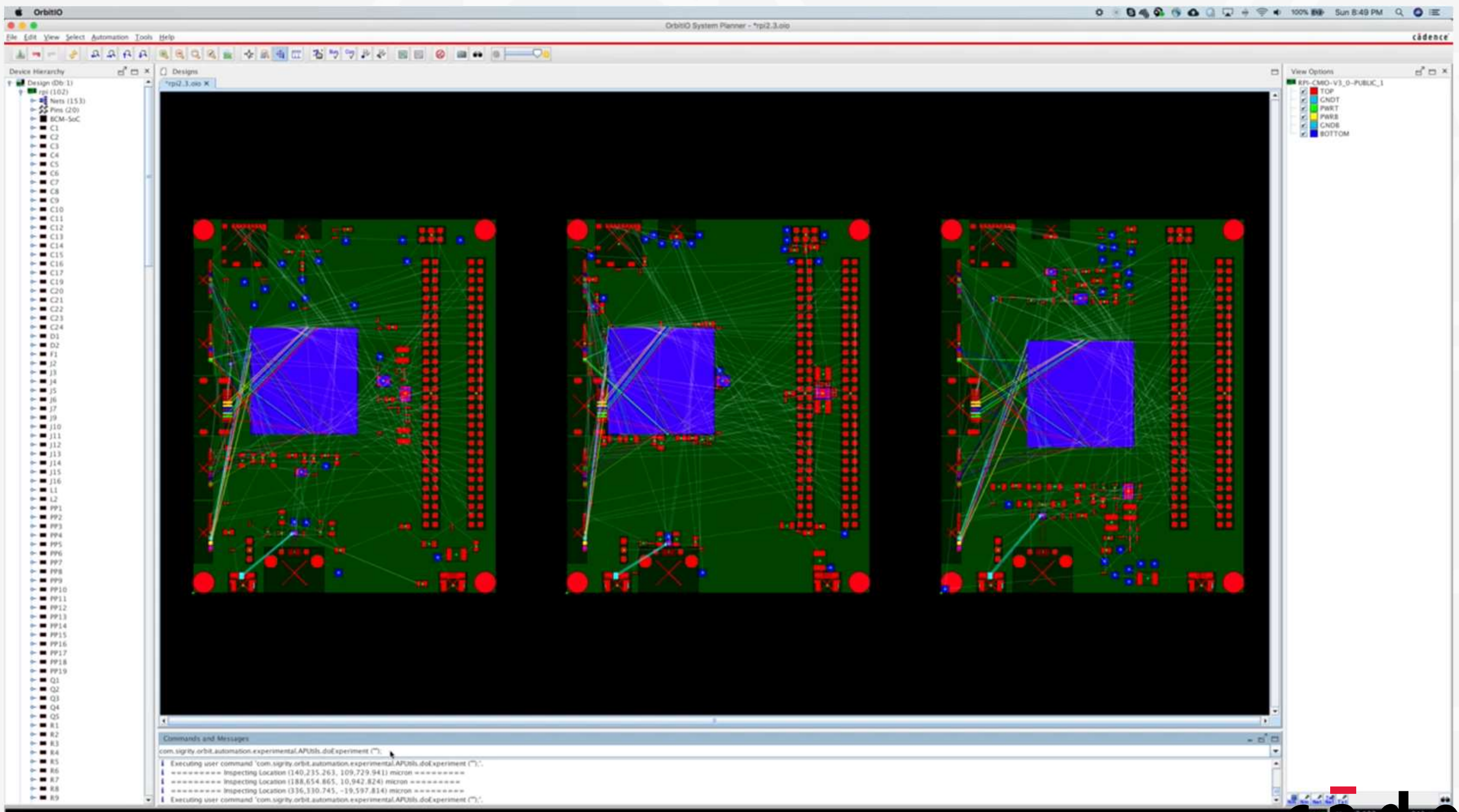
Distribution Statement A- Approved for Public Release, Distribution Unlimited

cadence®

LEARNING-BASED AUTOMATIC ROUTING OF PCB



LEARNING PLACEMENT FOR PCB IN ORBITIO DESIGNER



THE ELECTRONICS RESURGENCE INITIATIVE

ANDREW B. KAHNG

UC SAN DIEGO

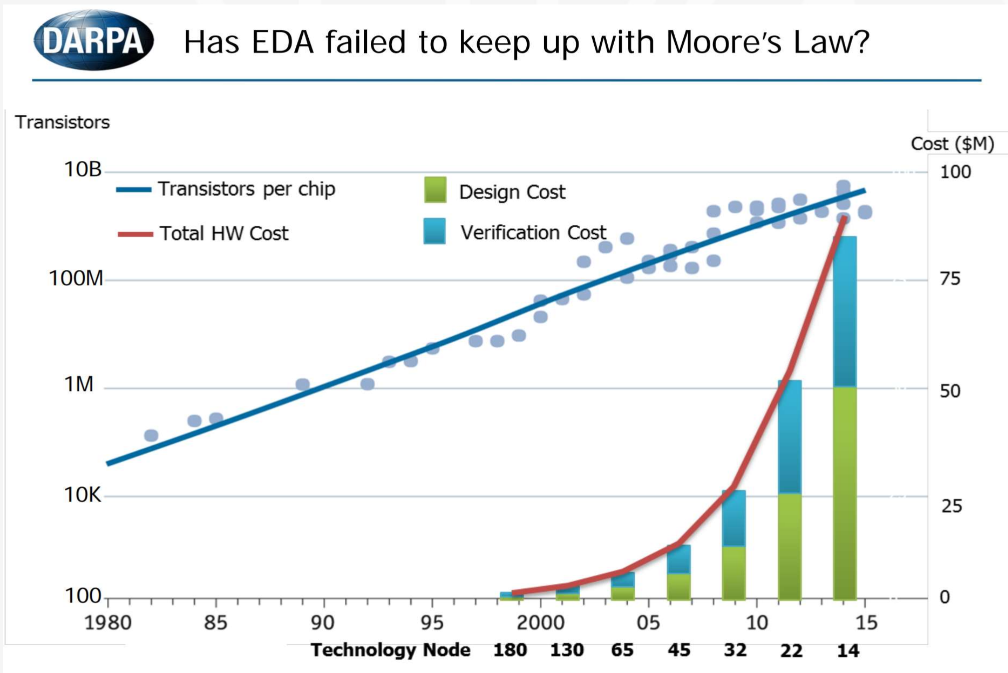
OpenROAD: Foundations and Realization of Open, Accessible Design

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA)

The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government

THE DESIGN CHALLENGE

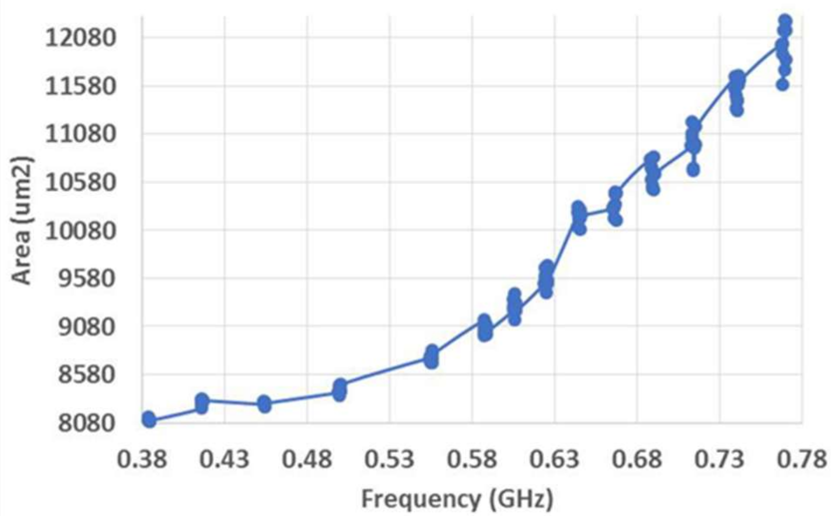
- Enormous barriers to hardware design in advanced technologies: Cost, Expertise, Unpredictability

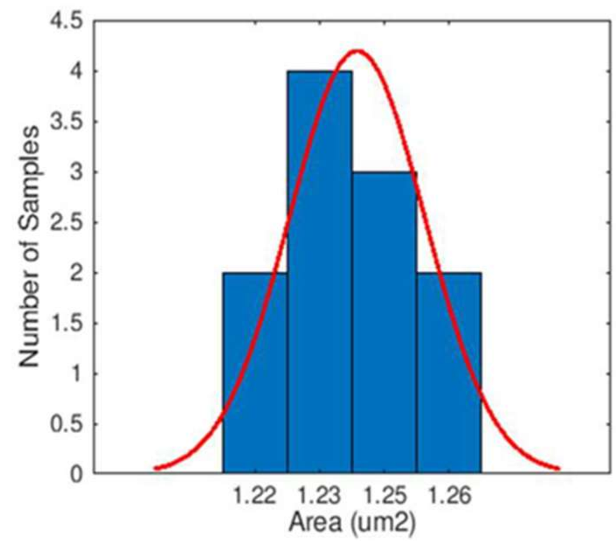


Source: DARPA

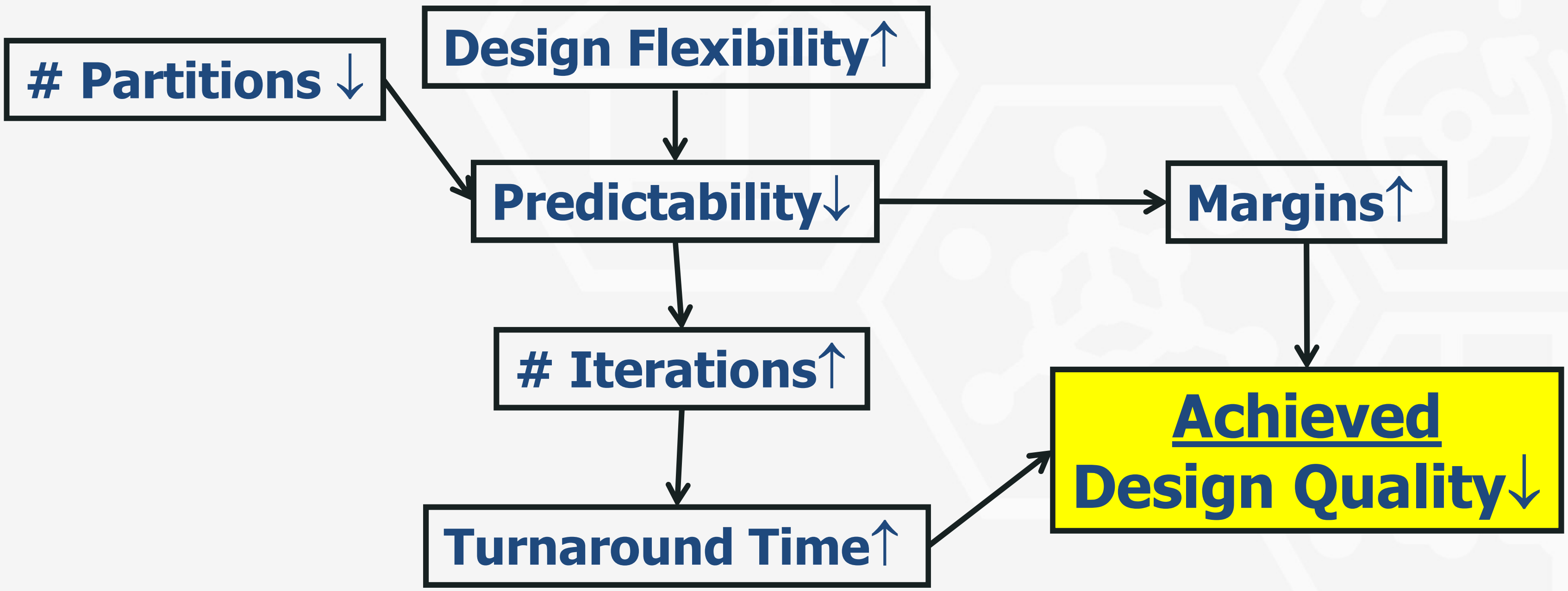
HOW IS IT DONE TODAY?

- Hardware design tools have evolved into complex “Swiss army knives”
- Chaos when tools are forced to “try hard”





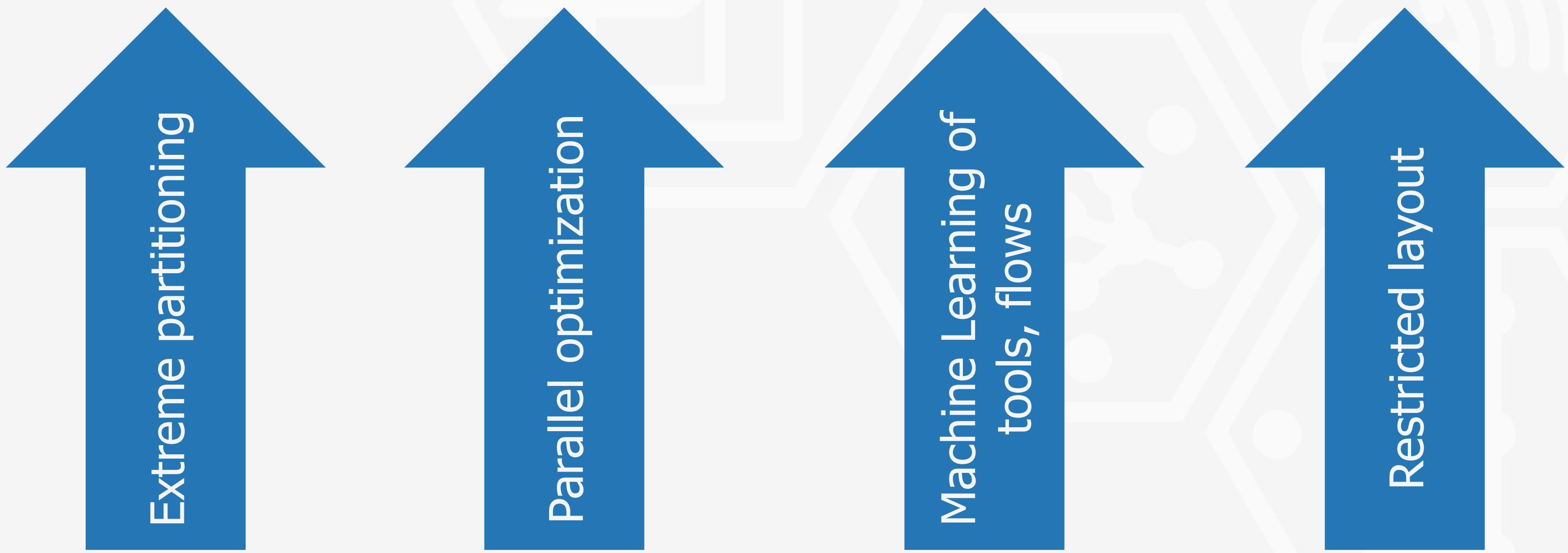
"LOCAL MINIMUM" OF HW DESIGN



Today: in a "local minimum" of design technology, methodology, and quality

NEW IN OUR APPROACH

24 hours, no humans – no PPA loss

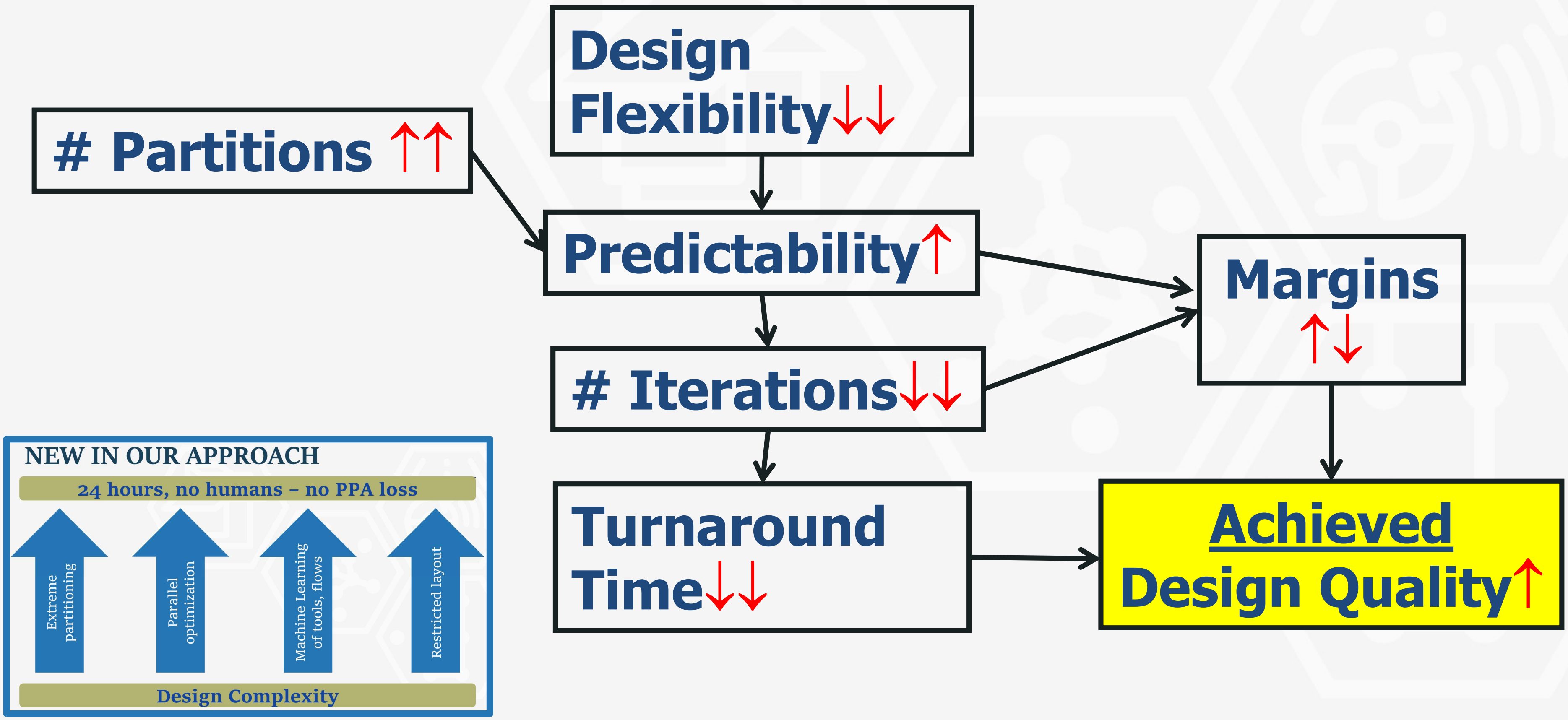


Design Complexity

FOUNDATIONS OF OUR APPROACH

- No Humans: tools must adapt and self-tune, must never get stuck unexpectedly
- 24 hours: extreme partitioning of problems
  + parallel search on cloud
  + machine learning for predictability
- Mantra: Correctness and safety by construction
- Mantra: Embrace freedom from choice

A NEW DESIGN PARADIGM



TECHNICAL CHALLENGES

- Data: small and expensive!
- Humans: are in the loop for good reasons!
- Fundamental tradeoffs: analysis cost vs. accuracy, optimization effort vs. quality
- Activation energies: new sharing mindsets, open-source ecosystem

OUR GOAL

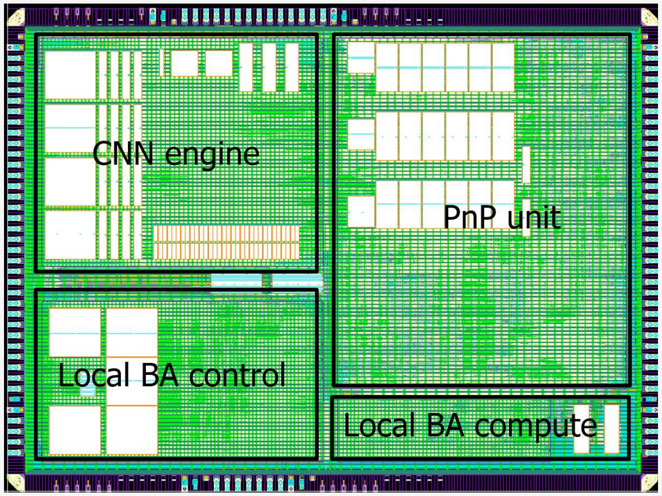
- 24-hour, No-Human-In-Loop layout design for SOC, Package and PCB with no Power-Performance-Area (PPA) loss
- Tapeout-capable tools in source code form, with permissive licensing → seed future "Linux of EDA"

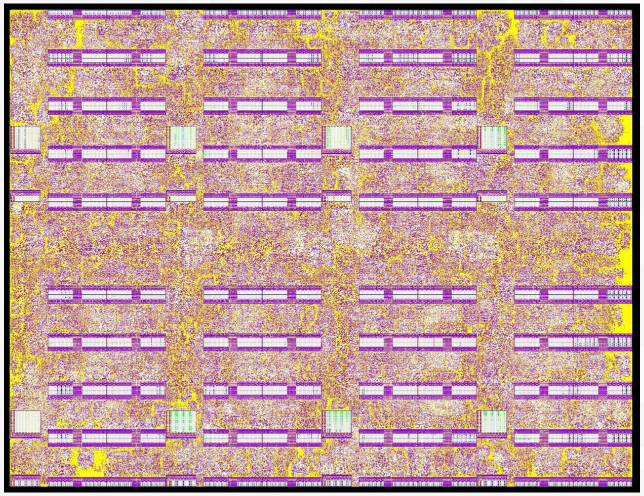
IMPACT IF SUCCESSFUL

- Create new “Base Technologies” that enable 24-hour, **autonomous** design
  - Extreme partitioning (bite-sized problems)
  - Parallel search and optimization
  - Machine learning: models of tools, designs
- New paradigm for design tools and methods: autonomy first
- Bring down barriers → democratize HW design

IMPACT ON DESIGN COST

- Embedded vision chips (28nm/16nm) from Michigan Internal Design Advisors team
- Layout @Michigan: 10+ weeks, significant resource
- OpenROAD and IDEA goal: 1 day, no humans (!)





SWINGING FOR THE FENCES

- Must achieve critical mass and critical quality

11 of 13 IDEA TA-1 subtasks
+ Base Technologies, Design

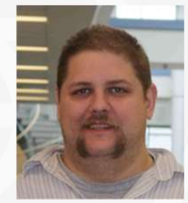
University of California - SD	Qualcomm
ARM	University of Minnesota
Brown University	University of Michigan
University of Illinois – UC	University of Texas - Dallas

Common Infrastructure		~~Databases / Processing~~	
	✓	Cloud Infrastructure	*Brown*
	✓	Timing Analysis	*UCSD*
	✓	Parasitic Extraction	*UMN*
	✓	Readers + Writers	*UTD*
	✓	Power and SI Analysis	*UMN*
Layout Generators	✓	Logic Synthesis	*Brown*
	✓	Floorplanning	*UIUC*
	✓	Placement	*UTD, UCSD*
	✓	Clock Tree Synthesis	*UCSD*
	✓	Detailed Routing	*UTD, UIUC*
	✓	Layout Finishing	*UTD, UCSD*
Design		~~SoC Design Advisors~~	

SWINGING FOR THE FENCES

- **Internal Design** team (Michigan)
  ~70 Ph.D., 50 M.S. graduates
  + 15 new SOC designs each year





- **Tools** team (UCSD, Illinois, UMinn, UT-Dallas, Brown):
  ~150 Ph.D., 80 M.S. graduates
  + many tools, engines "on the shelf"



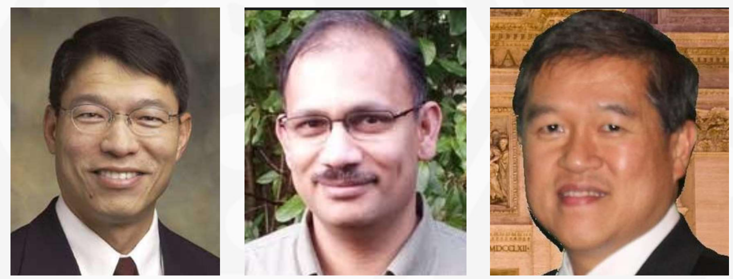
- **Qualcomm:** HW design, SOC-Pkg-PCB
- **Arm:** IP, system design + ML guidance



AND MORE …

Parallax software

- Open-sourcing of commercial timing engine
- Donated commercial tool source code base
- Industry advisors and technical contributors
  - Dr. Chi-Ping Hsu, Avatar
  - Dr. Noel Menezes, Intel
  - Dr. Richard Ho, Google
  - …



- Worldwide outreach, engagement, support …

National Taiwan University	Universidade Federal de Rio Grande do Sul	Seoul National University	Google	Avatar Integrated Systems
KAIST	CUHK	Intel	GLOBALFOUNDRIES	

THE ELECTRONICS RESURGENCE INITIATIVE

CLARK BARRETT

STANFORD UNIVERSITY

BREAKING BARRIERS IN FORMAL HARDWARE VERIFICATION

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA)

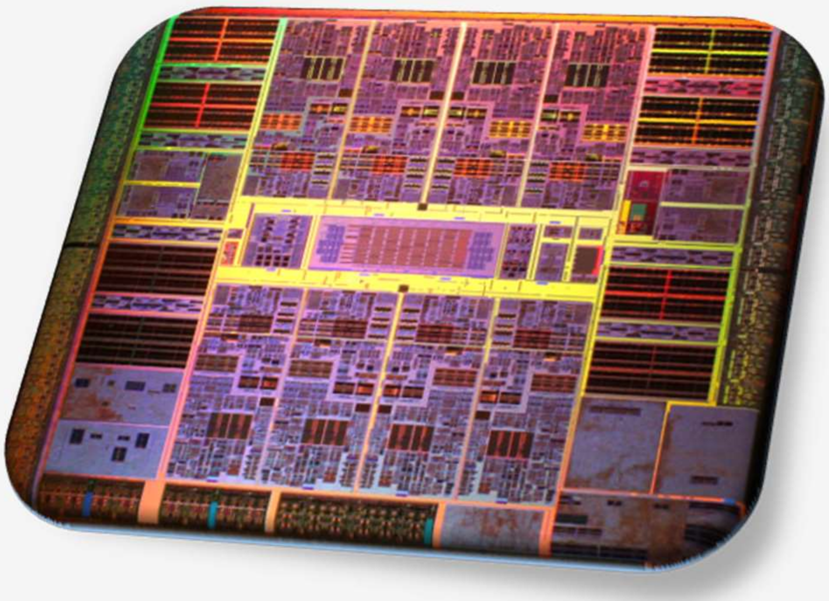
INTRODUCTION

THE NEED FOR BETTER VERIFICATION

THE VERIFICATION CHALLENGE

- Systems on a Chip (SoCs)
  - Growing in size and complexity
  - Single chip contains multiple cores, caches, accelerators

- SoC Verification
  - SoCs used in critical applications
  - Correctness is essential
  - Failures can be extremely costly (Intel FDIV: $500M)
  - Verification dominates design



THE VERIFICATION CHALLENGE

Verification takes roughly twice as long as all other pre-fab design activities combined

-Data from DARPA CRAFT proposer's day slide

Ultimately the reason I don't think it [open-source hardware] has taken root in the hardware community is verification.

-Bill Chappell in IEEE Spectrum Interview, July 16, 2018

FORMAL VERIFICATION

- Has potential to revolutionize verification
  - Better than testing: covers all possible cases
  - Already used extensively in industry
  - But there are many challenges

- Three main steps
  - Create a mathematical model of the system
  - Specify formally what the properties of the system should be
  - Prove that the model has the desired properties

FORMAL VERIFICATION

Upscale: Scaling up formal tools for POSH Open Source Hardware

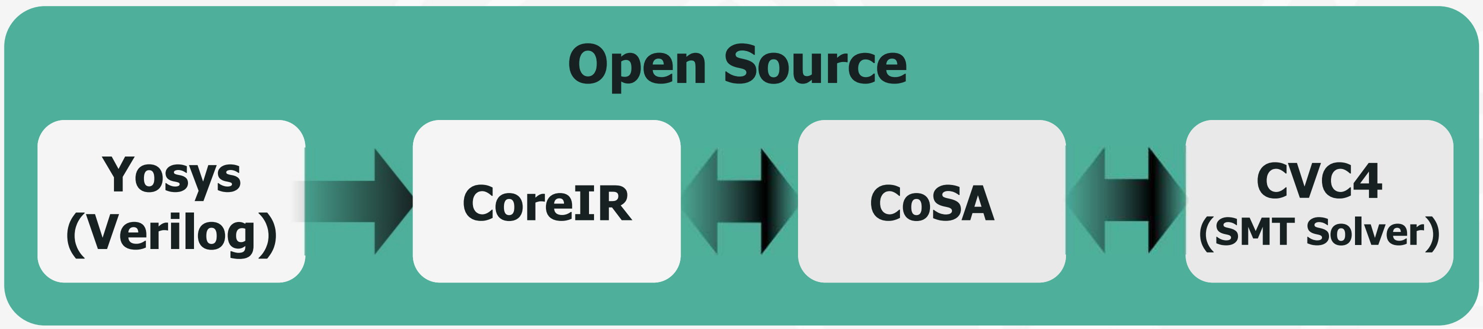
Clark Barrett, Mark Horowitz, Subhasish Mitra (Stanford)
Aarti Gupta, Sharad Malik (Princeton)

MODELING

MODELING

- Good news: HDL descriptions are already a formal model
- Challenges
  - Lack of non-commercial tools that can handle real designs
  - Analog / mixed-signal components
  - Closed-source IP can't be modeled precisely
- Solutions
  - Finally! - high-quality open-source toolchains are emerging
  - AMS circuits can often be approximated by digital circuits
  - New initiatives to build open-source hardware

UPSCALE OPEN-SOURCE TOOLCHAIN



- Yosys: open-source front-end for Verilog
- CoreIR: "LLVM for hardware" open intermediate representation
- CoSA (CoreIR Symbolic Analyzer): open-source formal analysis (model checking, bounded model checking)
- CVC4: open-source SMT solver

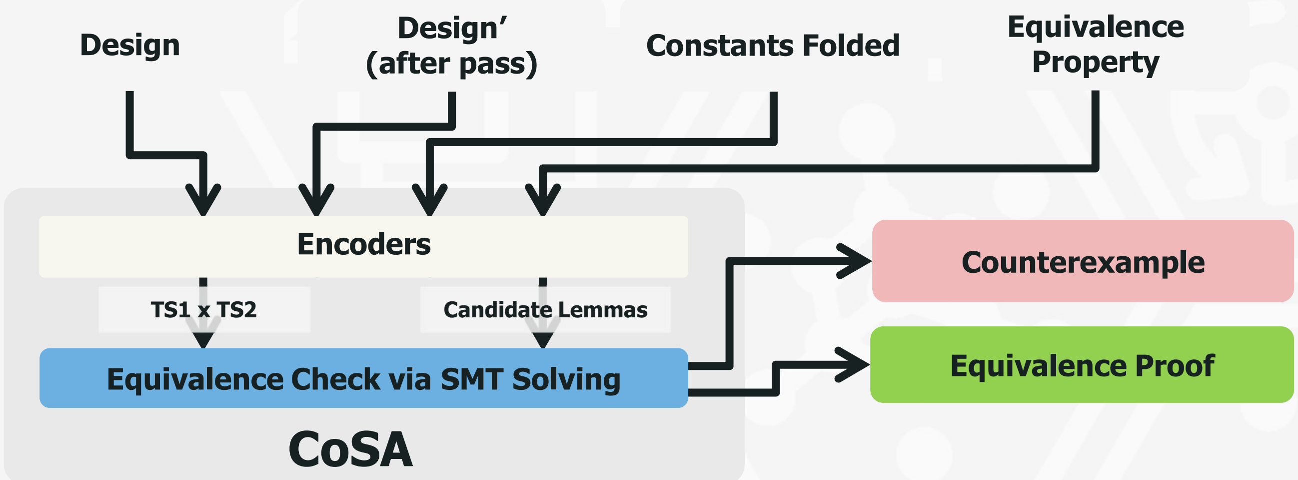
SPECIFICATION

SPECIFICATION

- Challenges for today's techniques (e.g. assertion-based verification)
  - Requires design knowledge
  - Requires manual effort
  - If incomplete, then will miss bugs

- Solutions
  - Integrated verification and design
  - Symbolic QED – no manual specification needed
  - Instruction-Level Abstraction – enables analysis of non-core SoC components

INTEGRATED VERIFICATION EXAMPLE: CONSTANT FOLDING



- Comparison of a CoreIR design before and after optimization pass
- CoreIR optimization pass provides information about constants folded directly to CoSA
- Significant performance improvement: 1.3 min vs. timeout (2 h)

QUICK ERROR DETECTION

- Quick Error Detection (QED)
  - Technique developed by Subhasish Mitra's group
  - Uses shadow registers and memory
  - Applies duplicate and check transformation to improve tests

	Regular	Shadow
Registers	R0-R15	R16-R31
Memory	0x10000-0x1FFFF	0x20000-0x2FFFF

```
...
LD R1,   [0x10000]
LD R2,   [0x10040]
...
```

```
LD R1,   [0x10000]
LD R2,   [0x10040]
LD R17,  [0x20000]
LD R18, [0x20040]
CMP R1 == R17
CMP R2 == R18
```

SYMBOLIC QUICK ERROR DETECTION

- Combines formal methods with QED
  - Leverages idea of self-consistency (Jones '96)
  - Does there exist *any* sequence of instructions that would fail a QED test
  - Searches all possible sequences using bounded model checking
  - Runs automatically overnight

- Early Results are promising
  - OpenSPARC T2: found 92/92 tough bugs automatically
    - Few minutes to few hours each
    - Each found bug returned a bug trace of less than 10 instructions
  - RIDECORE: (open-source out-of-order Risc-V core)
    - Automatically found previously unknown bug
    - Bug was reported and fixed

SYMBOLIC QUICK ERROR DETECTION

- Theoretical result: SQED is complete for large class of bugs
  - SQED can find essentially *all* bugs in processor cores
  - Limited only by the power of the bounded model checker

- Can be extended beyond processor cores
  - Same idea can be used for accelerators
  - Instruction-level abstraction (ILA) developed by Malik and Gupta (Princeton) makes accelerators look like processors

- Techniques for scaling up (work in progress)
  - Symbolic initial states
  - Automatic design partitioning
  - Abstraction of uninteresting components

PROVING

PROVING

- Challenges
  - Manual proofs require enormous effort
  - Automated techniques limited to small designs

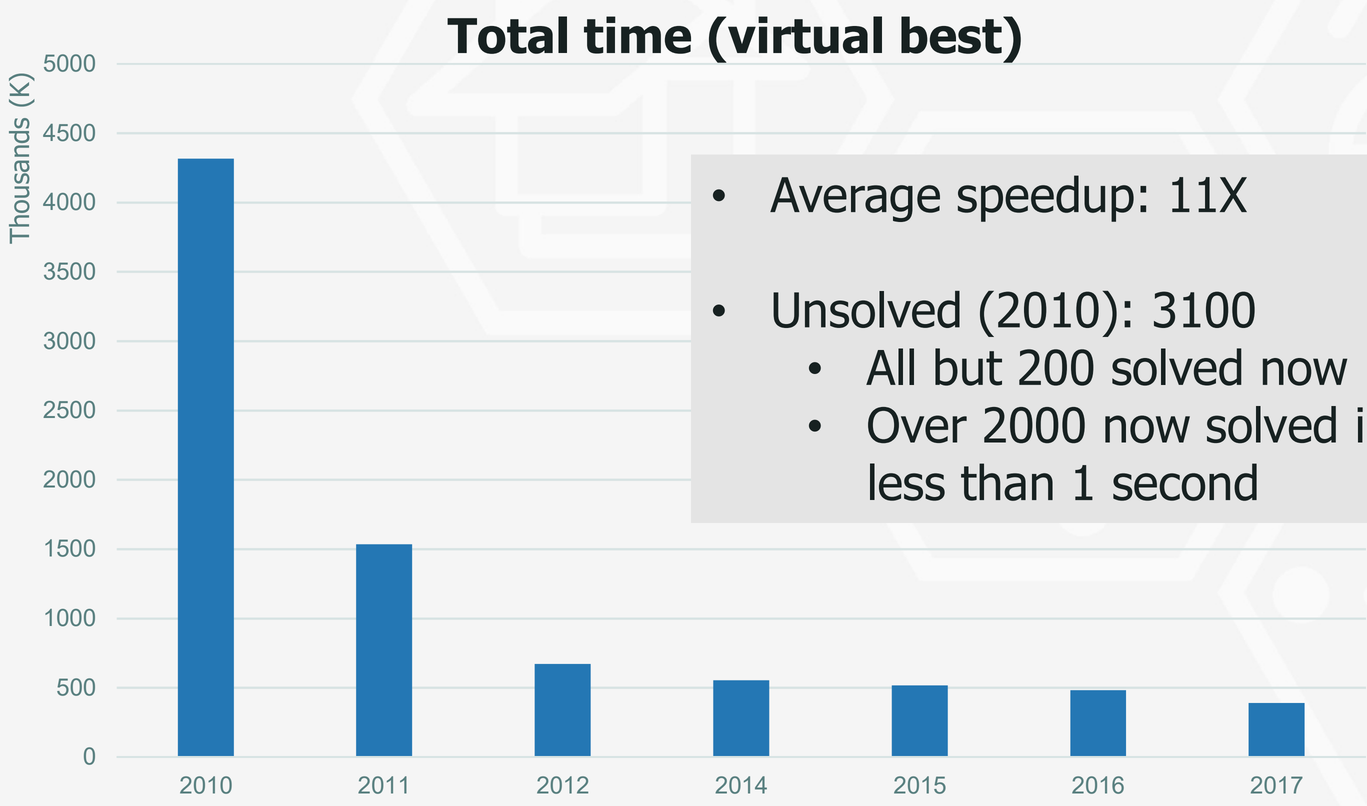
- Solution:
  - Better Solvers!

EVOLUTION OF SMT SOLVING

Quantifier-Free Bitvector (QF_BV) SMT-LIB benchmarks

- Comparison of virtual best SMT solvers since 2010
- Evaluation on 39610 benchmarks (SMT-LIB 2018)
- 41 different families of benchmarks

EVOLUTION OF SMT SOLVING



- Average speedup: 11X
- Unsolved (2010): 3100
  - All but 200 solved now
  - Over 2000 now solved in less than 1 second

THE ROAD TO EVEN BETTER SOLVERS

- Leverage Boolean satisfiability (SAT) technology
  - SAT solvers experiencing similar dramatic improvement

- Better SMT solvers
  - Lift SAT-based techniques to word level
  - Develop hardware-aware formal theories and solvers
  - SMT in the cloud – leveraging massive parallel computing
  - Machine learning for automatic solver tuning

CONCLUSION

- Tomorrow’s formal techniques will achieve unprecedented automation and scale
  - Innovation driven by open-source tools and hardware
  - New models for AMS
  - Integrated design and verification
  - Symbolic QED and Instruction-Level Abstraction for specification-free verification
  - Breakthroughs in back-end solver technology will drive larger and larger capabilities

THE ELECTRONICS RESURGENCE INITIATIVE

Distribution Statement A- Approved for Public Release, Distribution Unlimited

PETER
RYSER

SR. DIRECTOR – SOFTWARE & VALIDATION
XILINX, INC

SYSTEM VALIDATION FOR THE CLOUD AND BEYOND

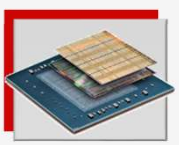
XILINX LEGACY: A HISTORY OF INNOVATION & INDUSTRY FIRSTS

World's First Fabless Semiconductor Company

World's First FPGA

First integrated processor in an FPGA

First HW/SW Programmable SoC



World's First 2.5D IC FPGA

First ASIC-Strength Design Suite

First Multi-Processing SoC (MPSoC)

SDx Development Environments

First RFSoC

Acceleration Stacks & Frameworks

"Firsts" Require High Quality

DRIVING ADAPTIVE COMPUTING WITH NEW DEVICE CATEGORY

ADAPTIVE COMPUTE ACCELERATION PLATFORM (ACAP)

Dynamically Adaptable to Workloads

> Adapts with programmable fabric

> Dynamic reconfiguration for diverse applications

Exponential Increase in Acceleration

> 20X AI compute capability

> 4X communication bandwidth for 5G

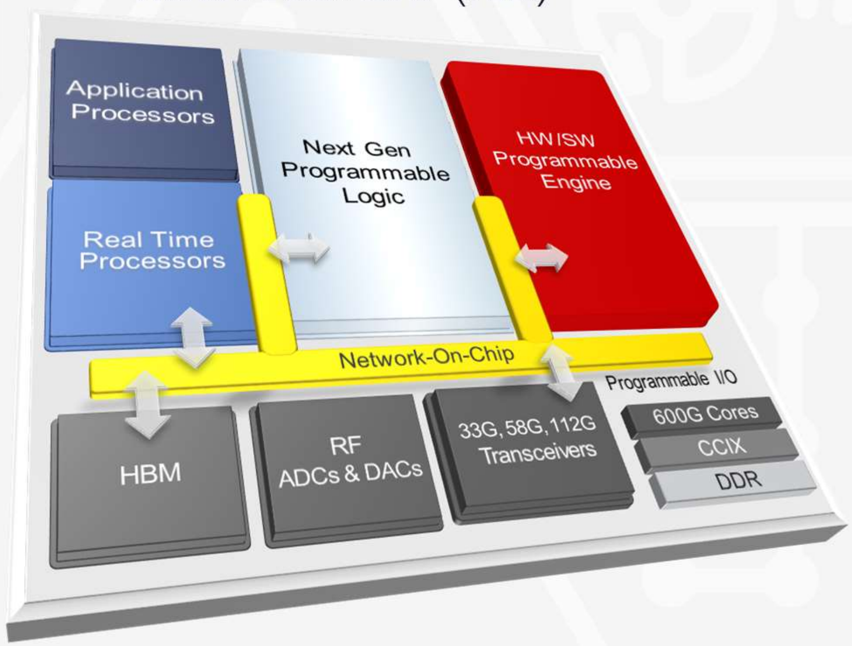
Fully Software Programmable

> Network-on-Chip & SW/HW accelerations engines

> Ease-of-programming for both HW and SW developers

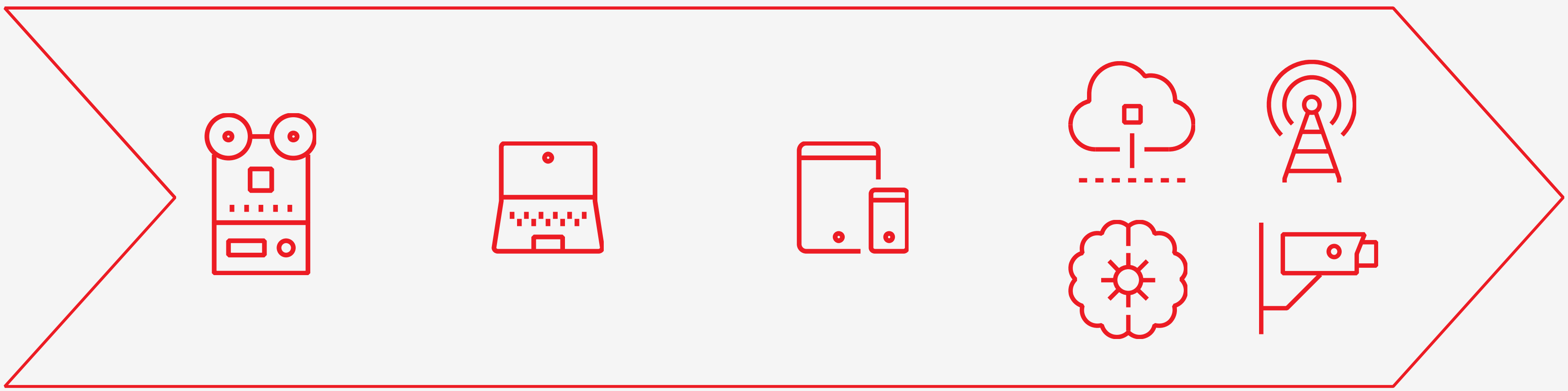
Project Everest

World's First ACAP (7nm)



THE EVOLUTION OF COMPUTING

Trend to Heterogeneous Architectures
with Acceleration of New Workloads in All Markets



Mainframe ERA

M's Units

PC Era

100M's Units

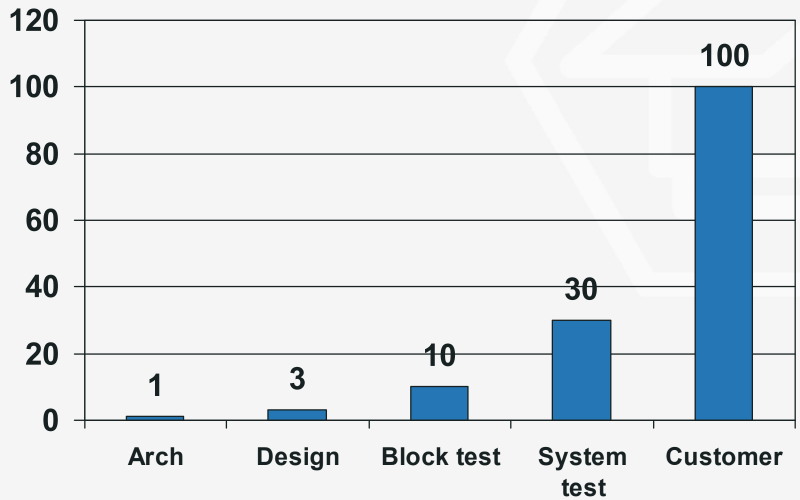
Mobile Era

B's Units

Pervasive Intelligence Era

50B Units

RELATIVE COST OF A BUG



- Bugs found late are costly
  - Hard to debug
  - Limited options to fix
  - Increasing mask costs
- Do more block and system testing much earlier in the development cycle
  - Test patterns
  - Software development and validation

Early Validation is a Key Enabler for a Successful Silicon Program

SW AND SILICON VALIDATION - SPEED VS VISIBILITY VS DEBUG

Emulator	
Execution Speed	~1 MHz
Tests/s	1
Aggregate Instructions/s	100
Visibility / Finds Issues	Great / Least
Cost per Bug	High

Multi-FPGA Prototyping	
Execution Speed	~10 MHz
Tests/s	10
Aggregate Instructions/s	75,000
Visibility / Finds Issues	Okay / Great
Cost per Bug	Medium

QEMU

Virtual Platform	
Execution Speed	500 MHz
Tests/s	500
Aggregate Instructions/s	5,000,000
Visibility / Finds Issues	Okay / Good
Cost per Bug	Low

Focus for POSH

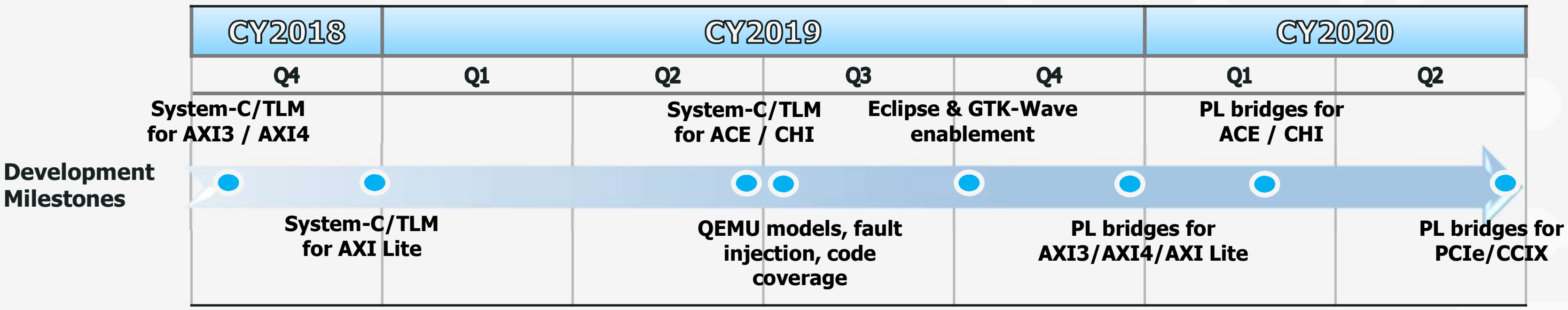
Silicon Validation	
Execution Speed	1.5 GHz
Tests/s	1500
Aggregate Instructions/s	15,000,000
Visibility / Finds Issues	Least / Best
Cost per Bug	Highest

Different Environments Offer
- Different Levels of Visibility
- Different Levels of Speed
- Different Levels of Debuggablity

Productivity Factors
- Easy migration of test cases between environments
- Build test systems out of the same RTL source base
- Run software as fast as possible
- Quickly root cause issues

XILINX & POSH

- Provide tools/mechanism for a fast, low-cost, system-level Simulation, Verification and Debug environment that includes Hardware and Software
- Use and enhance Open Source software (QEMU)
  - Build bridges for full system simulation
  - Co-simulate software and hardware
  - Support of heterogeneous systems
  - System-level debug



This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA)

SUMMARY

- Systems are increasingly heterogeneous
  - Mixing of traditional CPUs with accelerators
  - Connected together through the Cloud
- Verification space is rapidly expanding
  - Need to faster and better verify entire systems
  - Move the development and verification of accelerators to the software engineers
- Verification environments need to be flexible and connected
  - Not just at chip-level but at system and cloud level

THE ELECTRONICS RESURGENCE INITIATIVE

CHRIS TICE

VP, VERIFICATION CONTINUUM SOLUTIONS
SYNOPSYS

THE PETACYCLES CHALLENGE

REDEFINING EFFECTIVE HW VERIFICATION

CHRIS TICE
VP VERIFICATION CONTINUUM SOLUTIONS
SYNOPSYS

AUTONOMOUS DRIVING ESCALATES COMPUTING CYCLE NEEDS

Environment
Cameras, Radars, LiDARs

Position
GPS

Data
Cloud
V2X

Sensing and Perception

Sensing driving environment
Recognizing obstacle
Localization
Road detection

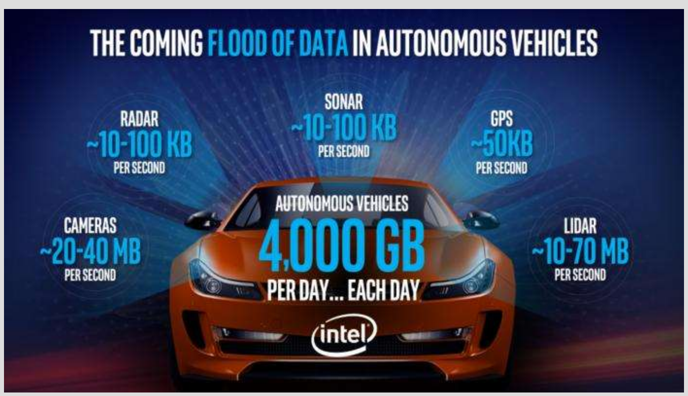
Planning

Recognizing environment
Making decision
Generating and optimizing path

Actuating

Visualizing

Autonomous Driving Scenario



+

Autonomous Driving Compute Requirements

>1,000,000 DMIPS

→

Autonomous Driving – ADAS

$5x10^6$ DMIPs @ 6 Cycles/ Inst

$30x10^{12}$ cycles/sec

3 minutes of ADAS

$5.4x10^{15}$ cycles

EXPANDING ELECTRONIC SYSTEM REQUIREMENTS

Driving Verification Challenges

Fast Growing Segments

Data Center & Edge

Automotive

IoT

5G Mobile

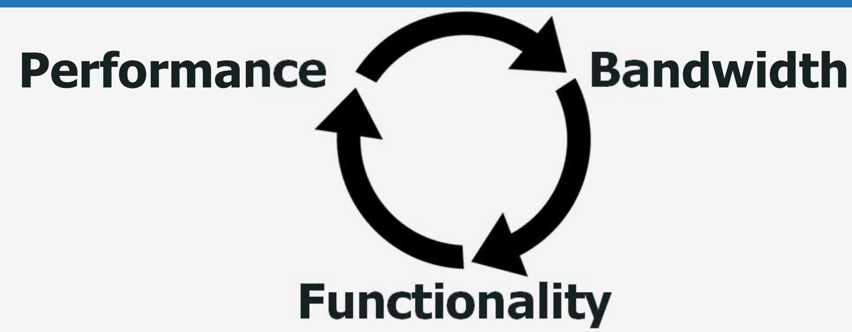
AI

EXPANDING ELECTRONIC SYSTEM REQUIREMENTS

Driving Verification Challenges

Fast Growing Segments

- Secure Real-time Computing
- Autonomous Vehicles/Drones
- Theatre Management
- Ruggedized Communication
- 3CI



New Challenges

- Ubiquitous Connectivity
- More Complex SoCs
- System Abstraction into SW
- Platform Hardening

EXPANDING ELECTRONIC SYSTEM REQUIREMENTS

Driving Verification Challenges

Fast Growing Segments

- Secure Real-time Computing
- Autonomous Vehicles/Drones
- Theatre Management
- Ruggedized Communication
- 3CI

New Challenges

- Ubiquitous Connectivity
- More Complex SoCs
- System Abstraction into SW
- Platform Hardening

TTM Goals Require Shift-Left Solutions

Integrity, Safety, Security

System & SW

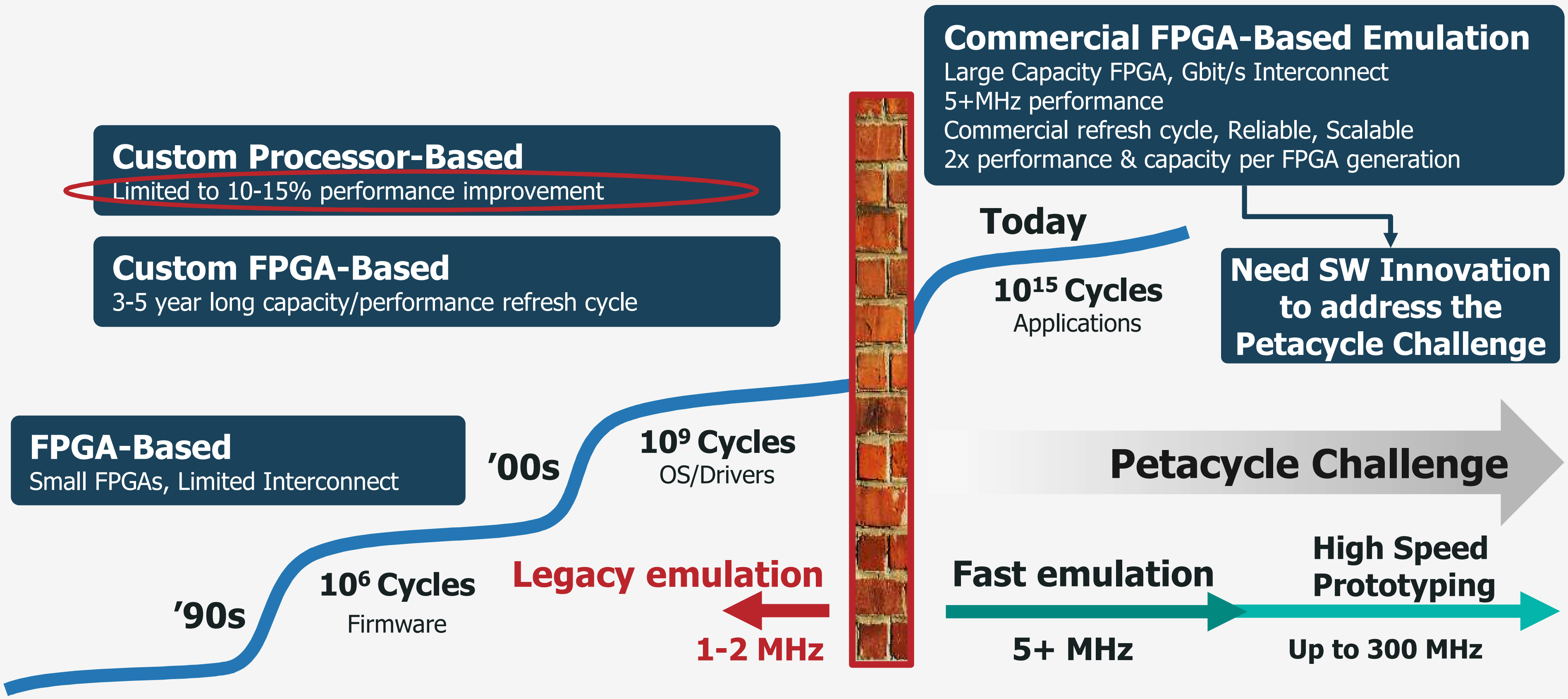
Verification

Design

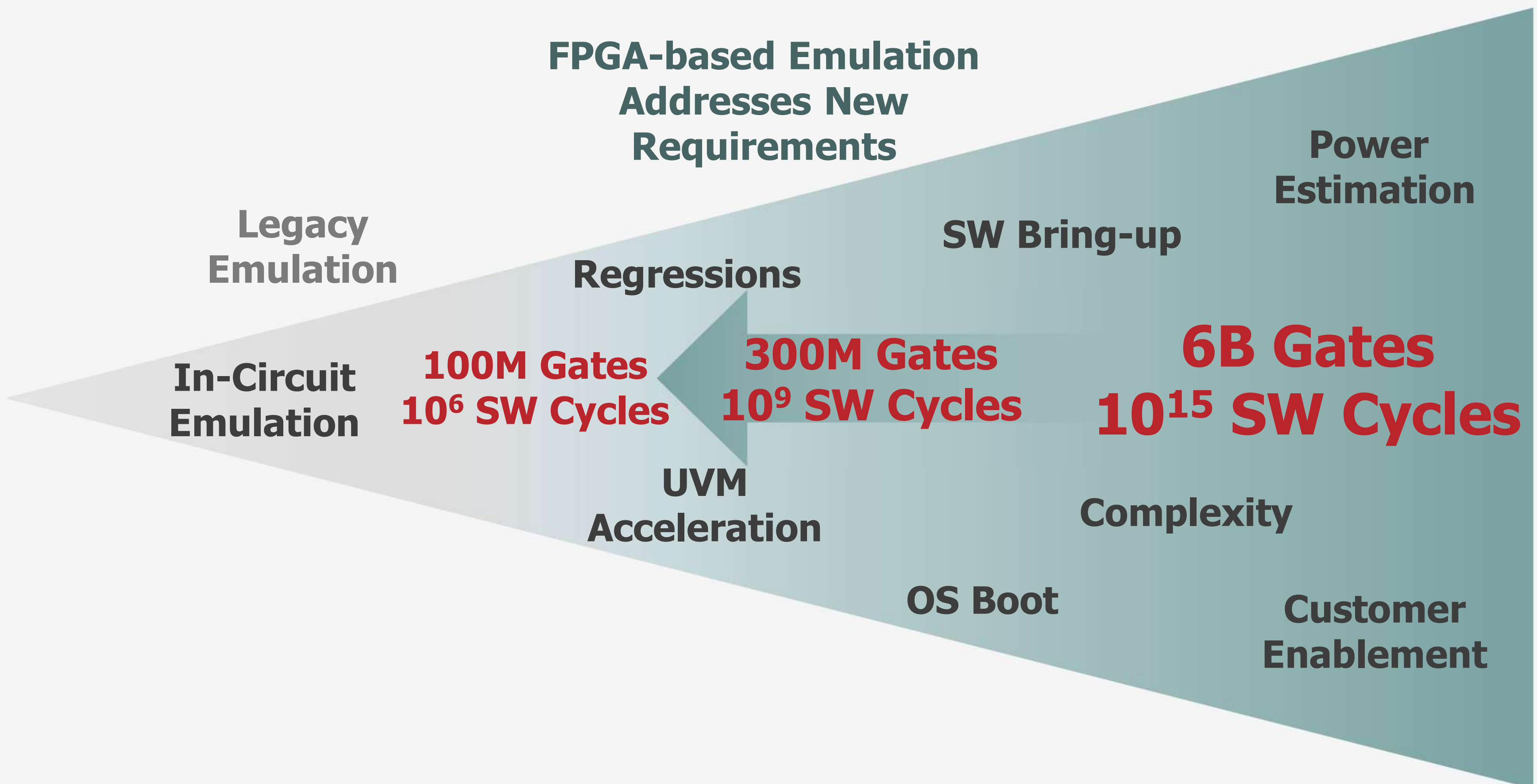
Expanding Scope: Schedules Shift Right

ADDRESSING THE SW CYCLES GAP

Redefining Emulation to Address Growing Software Content



FPGA-BASED EMULATION ENABLES PETACYCLE WORKLOADS



Distribution Statement A- Approved for Public Release, Distribution Unlimited

POSH NEEDS AND SYNOPSYS TECHNOLOGY SOLUTION

Need

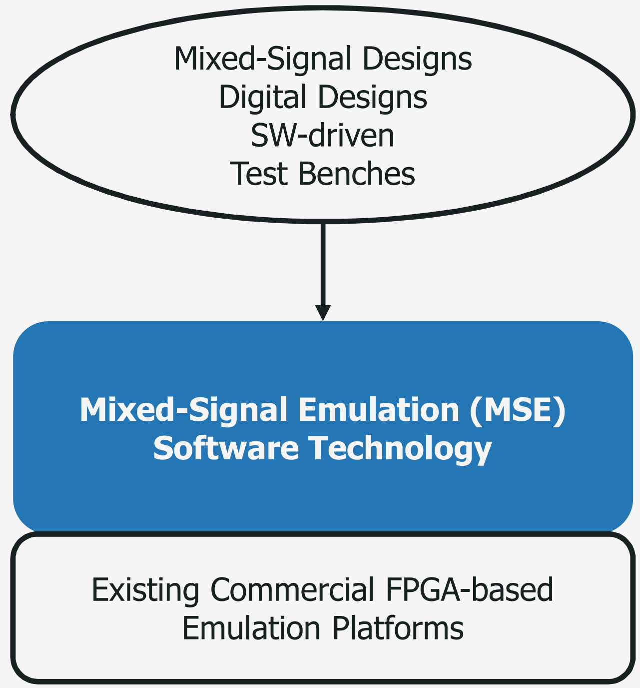
- Efficient early software bring-up & verification of Analog Mixed-Signal SoC designs

Novel Mixed-Signal Emulation Solution

- New mixed-signal methodology
- New set of emulation SW technologies
- Achieves MHz+ speeds on existing commercial FPGA-based emulation HW

Scalable Technology

- Converging digital & analog IP/SoC designs into emulation HW for **100x** performance gain vs. simulation



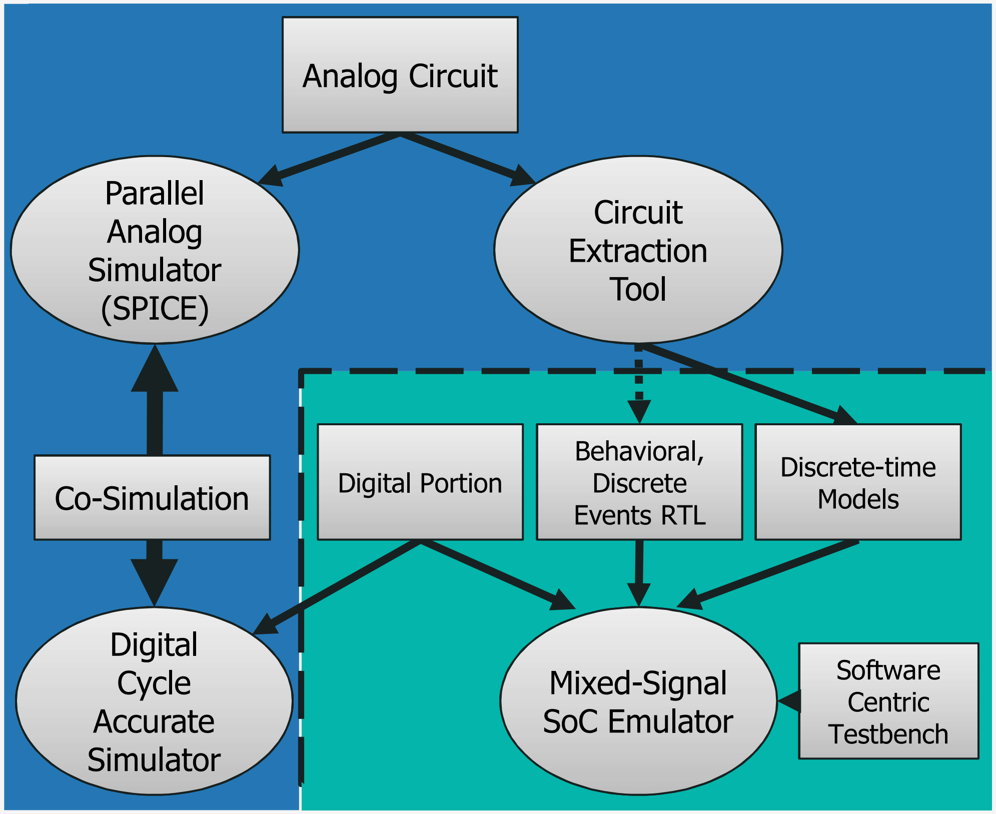
POTENTIAL ANALOG SOLUTIONS

Existing Verilog AMS co-simulation flow

- Co-simulation: Analog solver and digital simulation kernel run side-by-side

Proposed AMS technology

- SPICE netlist conversion to real number model (RNM) / discrete time digital approximation
- RNM emulation software tool & methodology (RNM already supported by VCS)
- Automatic AMS assertion generation



LEADERS TEAM UP TO ADDRESS POSH PROGRAM

SYNOPSYS®

Primary

Lockheed Martin

Sub-contractor

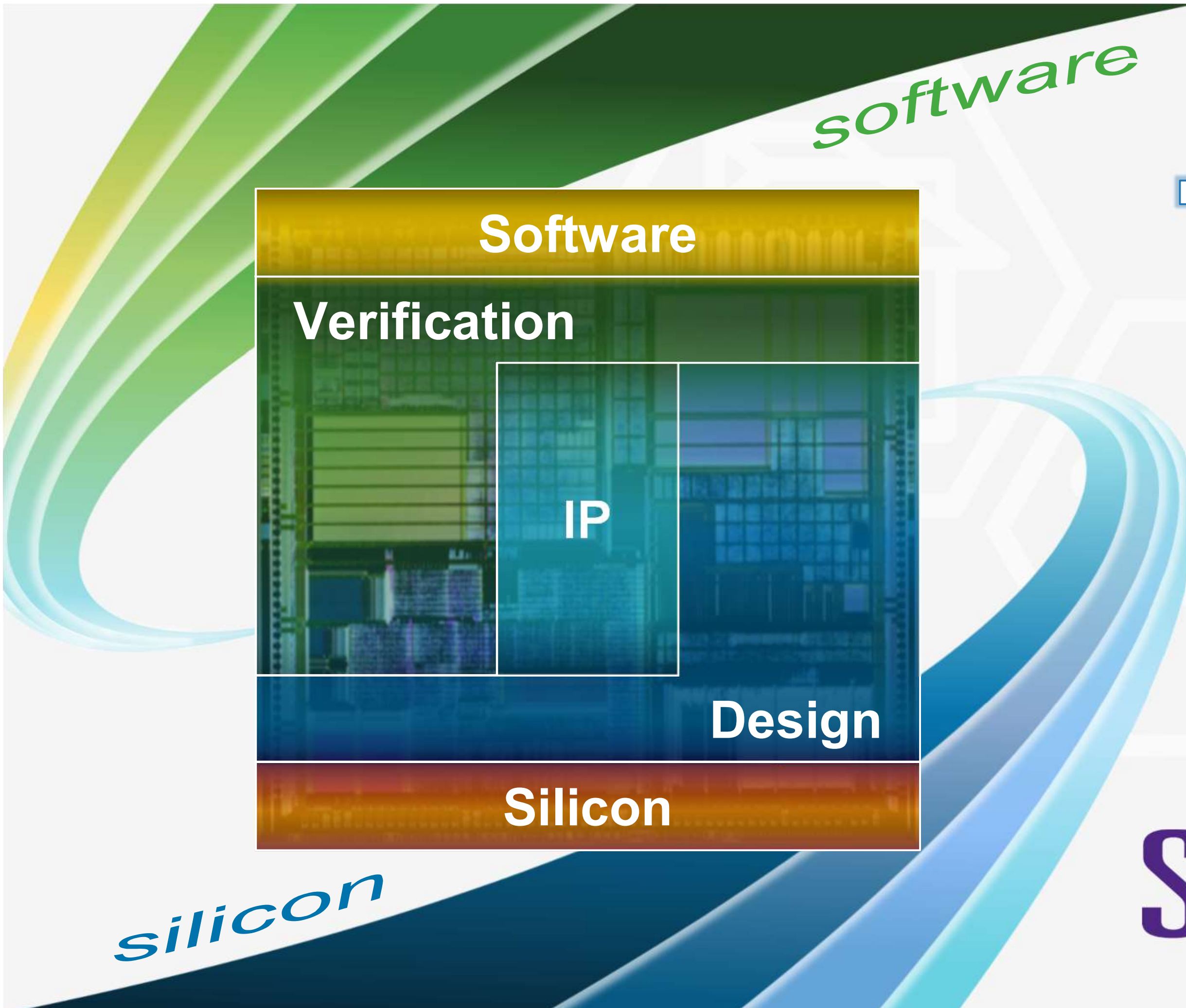
Analog Devices

Sub-contractor

Analog Circuit Works, Inc

Consultant

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA)



Thank You

SYNOPSYS®

THE ELECTRONICS RESURGENCE INITIATIVE